MODELING, DESIGN, FABRICATION AND DEMONSTRATION OF 3D IPAC GLASS POWER MODULES

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MODELING, DESIGN, FABRICATION AND DEMONSTRATION OF 3D IPAC GLASS POWER MODULES

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Dedicated to my parents and sister

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SUMMARY

The advent of smart and wearable systems along with their Internet of Things (IoT) applications are driving unparalleled product miniaturization and multifunctional integration with computing, wireless communications, wireless healthcare, security, banking, entertainment, and navigation and others. This evolution is primarily enabled by the integration of multiple technologies such as RF, analog, digital, MEMS, sensors and optics in the same system. Integration of these heterogeneous technologies creates a new need for multiple power supply rails to provide device-specific voltage and current levels. Hence, multiple power converters, each requiring several passive components, are used to create stable power-supplies. However, state-of-art power supplies employ SMD passives that are relatively large, forcing these modules to be placed on the board far from the active IC. This leads to significantly sub-par frequency performance and poses a challenge for ultra-miniaturized and reliable power supplies. Hence, novel packaging technologies that can improve miniaturization, electrical performance and reliability at a relatively low-cost are required to address these challenges. Georgia Tech-PRC proposes 3D integration of passives and actives (3D IPAC) as doubleside thin components on ultra-thin glass substrates with through-package-vias (TPVs) to meet these requirements. This thesis focuses on a comprehensive methodology to demonstrate a 3D IPAC power module, starting with modeling, design, fabrication and characterization to validate 3D integrated ultra-thin inductors and capacitors in ultra-thin substrates. Another key focus of this thesis is to advance building block technologies such as thinfilm inductors and capacitors to achieve the target properties for 3D IPAC integration.

As a first building block technology, advanced capacitor technologies were explored with high-k thinfilm barium strontium titanate dielectrics and lanthanum nickel oxide electrodes as an alternative to Cu, Ni and Pt electrodes for improved performance and cost. The BST capacitors with LNO electrodes resulted in a capacitance density of 20-30 nF/cm^2 with leakage as low as nA/nF up to 3 V. A glass-compatible process was developed with crystallization temperatures less than 650 C. These capacitors with thinfilm electrodes and dielectrics can be integrated into ultra-thin interposers and packages. This can help improve the capacitor performance up to the GHz range.

As a next build block, Si-nanowires were studied as high surface area electrodes for high-density capacitors. Analytical modeling was performed to understand the length of the nanowires based on the catalyst size. This modeling study was then extended to understand the cut-off frequency of the capacitors based on the RC time constant. The wires were fabricated using both chemical vapor deposition (CVD) and wet-etch processes. However, it was noticed that the wet-etch process provided more control on the geometry, density and orientation of the nanowires. Si-oxide was thermally grown on the surface of the wires. A capacitance density of 200 nF/mm^2 was achieved. It was noticed that the cut-off frequency of such capacitors was limited to the lower kHz range. However, the operating frequency can be improved by simply using a highly conductive Si-substrate.

The second part of the thesis focuses on inductor and capacitor integration on ultra-thin glass substrates for high-frequency power modules using the 3D IPAC

approach. Analytical models were used to calculate the required passive component values based on the target frequency, ripple currents and voltages of the power module. Next, a SPICE model was used to optimize the value of the required passives based on the output parasitics. The L and C structures were then modeled using 2.5D method of moments (MOM) approach. The modeling results showed 7-8 X improvement in Q-factor when the structures were fabricated using the 3D IPAC approach relative to those fabricated on the same side of the substrate. A fabrication process flow was designed based on through-via and doubleside metallization with semi-additive patterning (SAP). The components were fabricated as thinfilms on either sides of the substrate and interconnected with through-vias. The LC network was characterized using a two-port vector network analyzer. The results showed low-pass filter response, which matched the design targets of cut-off frequencies upto 100 MHz. This study, therefore, demonstrates advanced thinfilm component technologies for ultra-high frequency power-supply. It also presents, for the first time, a 3D integrated passives and actives (3D IPAC) approach with integrated L and C for power modules.

CHAPTER 1

INTRODUCTION

1.1 Introduction:

Smart and wearable electronic systems that provide computing, wireless communications, wireless healthcare, security, banking, entertainment, navigation, and a variety of other functions are emerging as the key future technology drivers. Providing such a myriad of functions in such portable systems requires the integration of multiple functions such as digital, RF, analog, optics, MEMS and sensors devices into ultra-small systems, each requiring specific current and voltages for their optimal performance, resulting in the need for multiple power supply rails [1-5].

Typical power converter modules consist of an active PMIC (power management integrated circuit) along with input decoupling capacitors, storage inductors and output filter capacitors [6]. Most state-of-art power management modules consist of a PMIC and an application processor assembled side-by-side on an organic board with multiple passive components. Such modules that are present in Samsung's Galaxy S3 and Apple's iphone 6 smartphones need to be enhanced for next generation because of their large parasitics and large real estate they take on the board. Fig. 1.1 shows leading smartphones from Apple with PMIC and SMD passives assembled side-by-side [7].

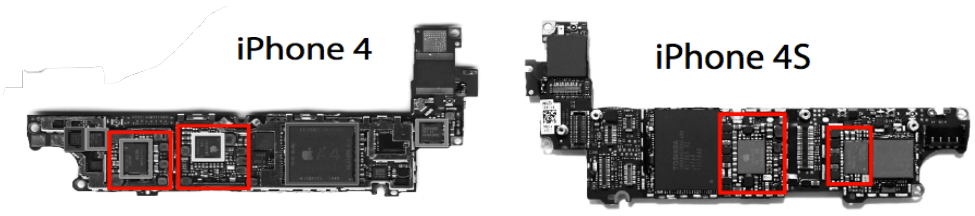


Fig. 1.1: Apple's iPhone 4 and 4s with PMIC and passive components mounted side-by-side in separate packages [7].

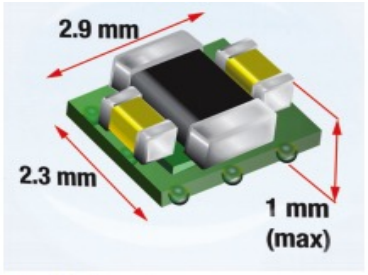


Fig. 1.2: TI's MicroSIP module with embedded die and SMD power components [8].

The trend for increased miniaturization with higher power is leading to the development of integrated solutions. Such systems have both the PMIC and the passive components assembled together to form a functional module leading to improved power delivery over current state-of-art. The TI microSIP[8] is one of the most area-efficient commercially available modules today. It uses an ultra-thin Si die embedded in an organic core with power components mounted on the top. An image of this is shown in Fig. 1.2. It consists of an embedded PMIC in an organic core and surface mount components on the top. The passives comprise of a large inductor in the center and two capacitors assembled on either side. There are two smaller components, which are the input, and output capacitors and the larger component is the output inductor. These systems employ SMD components that are 100s of microns in thickness. This forces them to be mounted relatively far from the active IC leading to sub-par frequency performance. Integrating components closer to the IC can significantly help improve the frequency performance of these devices.

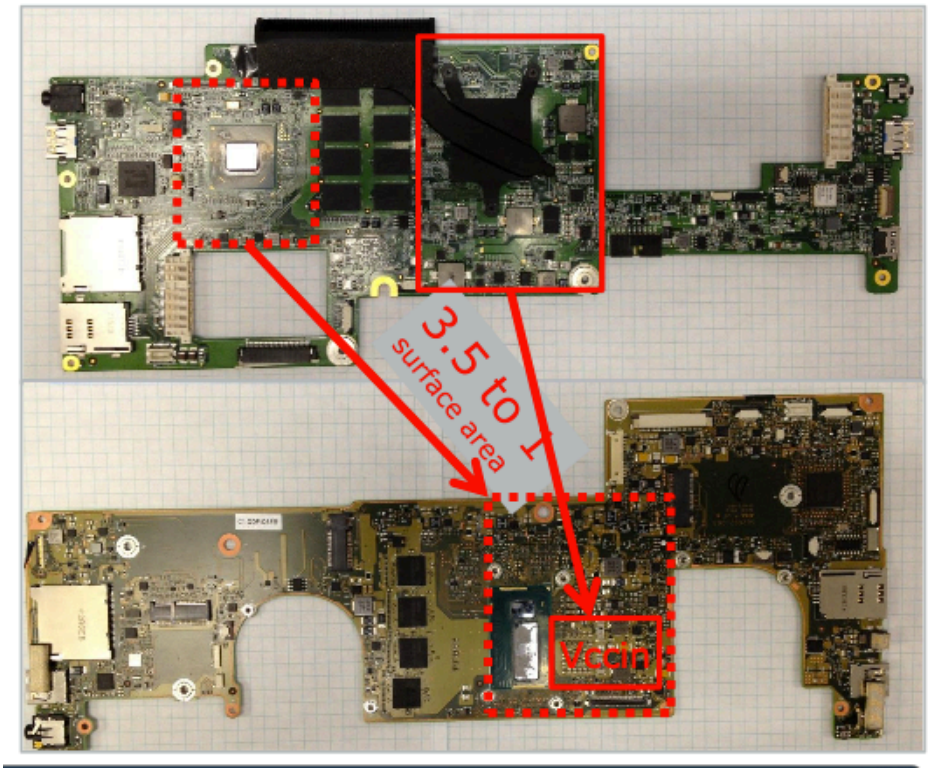


Fig. 1.3: Space reduction by 3.5X when moving from power modules with SMD passives in IVY Bridge (top) to FIVRs with integrated board-level inductors in Haswell processors (bottom)[9].

Another approach to save real estate and improve performance is seen in Intel's Haswell processors, shown in Fig. 1.3. Intel moved to a fully-integrated voltage regulator (FIVR) technology with their Haswell processors, eliminating as many as seven external PMICs. This architecture allowed for smaller inductors and capacitors and as much as 75% fewer components resulting in a 3.5 X less surface area, 2 mm thinner board and frees up real estate for a 10% larger battery. However, several SMD components are still used as part of this architecture. These components are mounted on the board relatively far from the active IC when compared to the integrated inductors. This results in larger parasitics from the long interconnect lengths. This affects the overall frequency performance. Having IVRs complete with integrated inductors and capacitors can help mitigate this challenge

and significantly help improve performance. The inductors also require multiple layers on the PWB to achieve the required inductance densities.

On-chip power supplies offers many advantages over modules based discrete components and SiPs. They reduce PCB area and enable fine-grained voltage controls with precise voltage delivery, voltage scaling and improved frequency response. The ultrashort distance to the load leads to very low interconnection parasitics resulting in ~2000X faster scaling as compared to off-chip voltage regulators. However, their voltage and current are limited to a few volts and milli-amps.

The trend in power modules from discrete to partially integrated modules is illustrated in Fig. 1.4. This Fig. also shows the migration towards integrated 3D power modules with thinfilm components as the ultimate goal, with about 10X increase in power densities. Hence, advanced thinfilm component technologies with the best properties, and their integration into ultra-thin substrates are required to meet the emerging needs for performance and size.

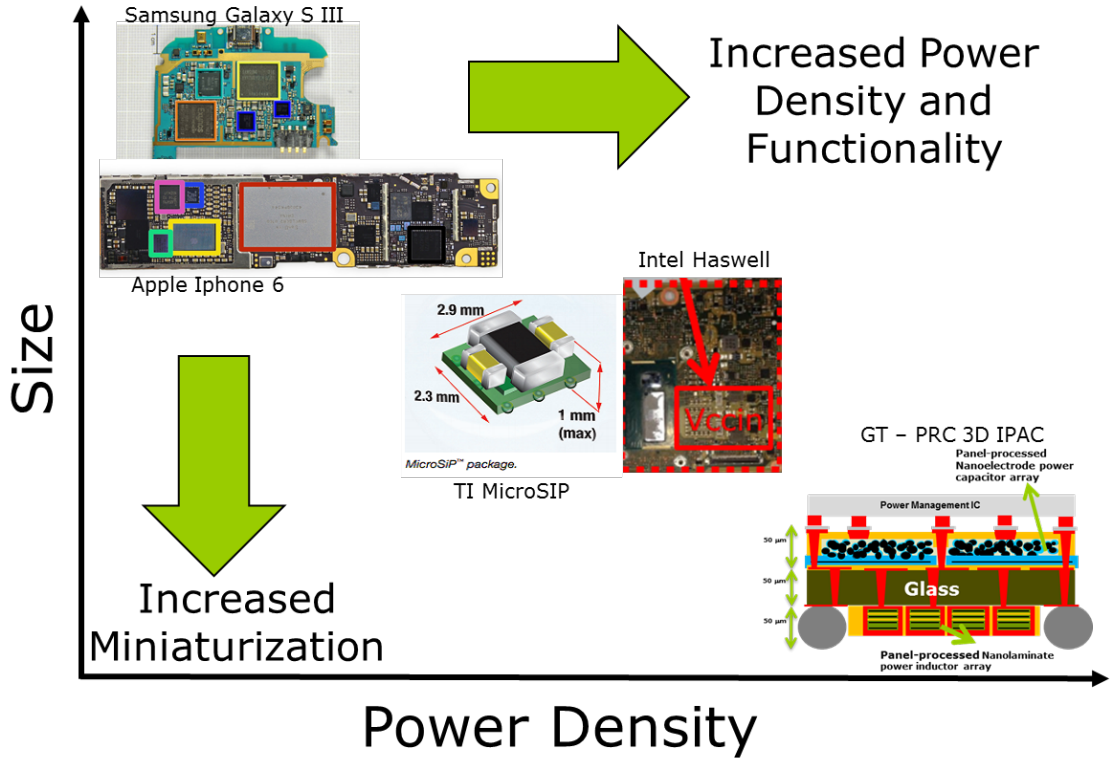


Fig. 1.4: Trends in power module miniaturization.

1.2 Research Objectives:

The primary objective of this research is to model, design, demonstrate and characterize miniaturized 3D IPAC power modules with ultra-thin high-density capacitors and inductors, with low interconnection parasistics for higher operation frequencies. Hence, demonstration includes the integration of inductors and capacitors on ultra-thin glass substrates with through-vias to form the complete ultra-miniaturized 3D IPAC Power module. The key research goals are benchmarked with prior art in Table 1.1a, 1.1b and 1.1c and summarized in Fig. 1.4.

Table 1.1a: Research goals: Advanced Capacitor Technologies

Parameter	Prior Art	Objectives	Challenges
High-k thinfilm Capacitors			
Capacitance Density ($\mu F/cm^2$) Leakage Current ($\mu A/cm^2$)	0.5 – 0.6 50	2 – 3 <5	Electrodes and processes
High-Surface area Capacitors			
Capacitance Density Frequency stability	20 $\mu F/mm^3$ < 50 -100 kHz	100 $\mu F/mm^3$ >200 kHz	Low-ESR electrodes and interfaces

Table 1.1b: Research goals: Advanced Inductor Technologies

Parameter	Prior-Art	Objectives	Challenges
Inductance Density (nH/mm^2)	10 – 20	40 – 80	High inductance and high Q at 100 MHz using a single RDL layer with low DC Resistance.
Q Factor	20	>35	

Table 1.1c: Research goals: 3D IPAC Power Modules: Integrated L and C

Parameter	Prior Art	Objectives	Challenges
Module dimensions (mm^3)	2.9x2.3x1	2x1x0.15	3D integration of ultra-thin components TPVs in glass
Loop Inductance (nH)	1 – 10	< 0.1	Interconnect length in Z and X-Y directions
Integrated Capacitor ($\mu F/cm^2$)	1 – 2	100	Ultra-thin component integration on ultra-thin substrates
Integrated Inductor (nH)	20 – 30 (Q <20)	80 (Q>35)	Integration using single layer RDL on ultra-thin substrates
Frequency (MHz)	1 – 2	>100	Component stability > 100 MHz

1.3 Technical Challenges:

Decoupling capacitors at the input, and filter capacitors and inductors at the output, form the key components in achieving a noise-free power supply. As the demand for higher switching speeds increases, the need to control parasitic inductance also becomes extremely important. The primary challenges with power conversion and delivery are the lack of critical energy storage components such as capacitors and inductors to supply power at low impedance in the required volumetric densities and form-factors, and their integration into ultra-miniaturized modules with both X-Y and Z shrinkage while retaining high performance. The research challenges are classified into these three categories:

1.3.1 Advanced Capacitor Technologies: The capacitance of a parallel-plate capacitor is calculated as:

$$C = \frac{A\varepsilon\varepsilon_r}{t} \qquad (1)$$

Where A = Surface area of the electrode, ε = Permittivity in vacuum, εr = Relative permittivity of the dielectric, and t = thickness of the dielectric. Ultra-high capacitance densities are achieved using three factors: Thin dielectrics, high-permittivity (k) dielectrics, and high-surface area electrodes. Advances in these such as by nano-structures, nano-dielectrics and processes invoke many challenges as discussed below:

1.3.1a Thinfilm Capacitors**:** Oxide thinfilm capacitors are easy to process with techniques such as anodization or sputtering but do not achieve adequate capacitance densities. High-permittivity dielectrics achieve 2-3X higher capacitance densities but require stable electrodes that can withstand high processing temperatures > 700 C. High-K thinfilm capacitors with barium strontium titanate as the dielectric typically use Pt electrodes with Ti or Ta as the diffusion barriers. Pt is an expensive material. Cu and Ni are ideal

electrodes but do not provide stable dielectric-electrode interfaces at high temperatures required to crystallize BST. This becomes a major challenge as post-annealing temperatures used to crystallize BST exceeds 700 C. Hence, achieving capacitance densities of 2 – 3 $\mu F/cm^2$ with leakage currents < 100 nA/μF and BDV of 10 V using low-cost electrodes and substrate-compatible processes are major challenges.

1.3.1b High-surface area capacitors**:** High-surface area electrodes require porous particulate or etched structures. Etched structures are preferred because of their compatible processes with a variety of substrates. Si- based trench capacitors have been explored, but have found limited applications because of the processing complexity with the Si etching, and dielectric and top-electrode depositions. Nanowires form high-surface area electrodes that can be considered to achieve ultra-high capacitance densities. However, the high ESR from electrode resistivity and wire geometries forms a major challenge for use in high-frequency applications.

1.3.2 Advanced Inductor Technologies: Surface-mount ferrite inductors are the workhorses for the power convertor industry. However, they are facing fundamental limitations in low frequency-stability and volumetric energy densities. They are also manufactured as thick components, which further limits their integration in emerging ultra-thin packages. Planar power inductors with thick and fine-pitch spirals or coils to achieve the required inductance densities with the desired Q in a single layer at low cost, are therefore preferred. Design of such high-Q power inductors with 20-50 nH/mm^2 and Q factors of 20-30 with the required performance and processability is another major challenge. Magnetic thinfilm inductors increase the inductance densities over planar inductors but face challenges associated with processing and degradation in quality factors.

1.3.3 Ultra-miniaturized power modules with integrated L and C:

1.3.3a Electrical Modeling and Design Challenge**:** Package-level electrical modeling and design with low loop inductance and low plane resistance, requires optimization of: 1.) the number of vias interconnecting the different components and 2.) Via location to minimize the loop inductance. Another challenge arises from optimizing the metal plane thicknesses to address the trade-offs between parasitic resistance and inductance. Solving the above challenges is important to achieve stable high-frequency performance.

1.3.3b Complete module fabrication challenge with integrated L and C: The realization of a complete module requires the development of multiple building block technologies such as high-density capacitors and power inductors that are compatible with substrate build-up processes. Fabrication of the module with ultra-thin (30 – 100 μm) substrates with through-package vias (60 μm), thinfilm component integration and IC assembly adds several fabrication concerns.

a. High-density capacitors require a set of electrodes that are not easily compatible with standard build-up processes. Novel processes are required to integrate such capacitors.

b. Another key challenge is integrating these two disparate fundamental building block technologies onto one ultra-thin substrate, interconnected by through-vias to form a complete power module.

1.4 Proposed Unique Approach

A novel 3D IPAC concept is being pioneered by GT-PRC to comprehensively address the component and module integration challenges for ultra-miniaturized and high-performance systems. The 3D IPAC structure consists of an ultra-thin (30-100 microns) low-loss glass substrate, low-cost through-package vias (TPVs) and double-side RDL. Both passive and active components can hence be integrated on both sides of the glass substrate, either as thinfilms or discretely fabricated and assembled components. Fig. 1.5 shows the schematic of the 3D IPAC structure. The ultra-thin glass substrates with TPVs enable ultra-short interconnections between the active and passive components. This ensures low loop inductance and improved frequency response.

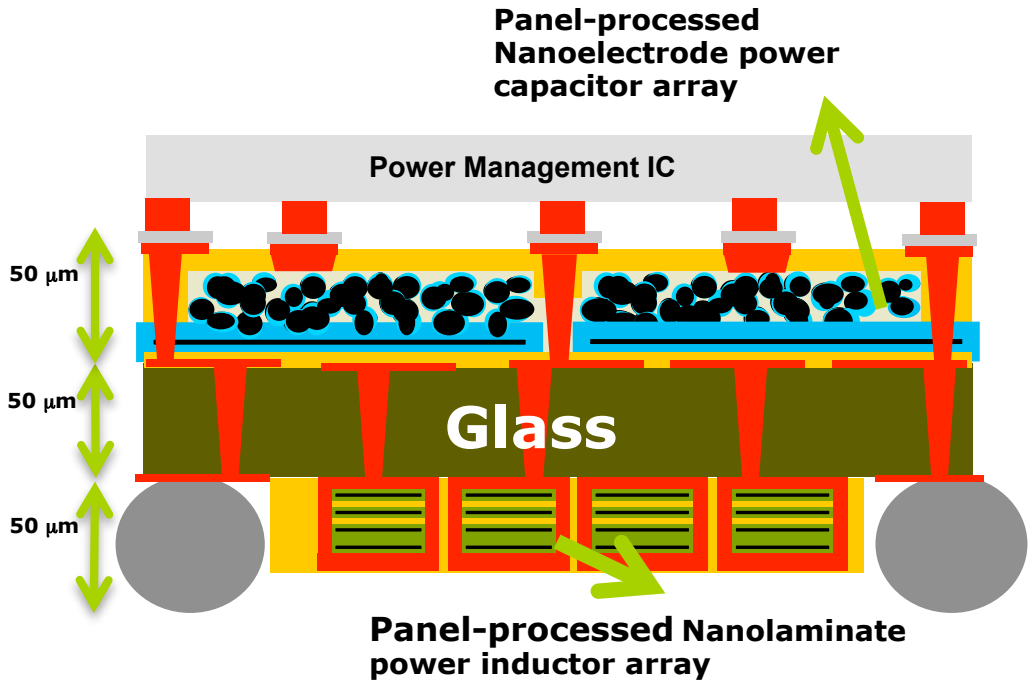


Fig. 1.5: Schematic cross-section of 3D IPAC power module with integrated L and C.

To realize the 3D IPAC concept for power, several advances in thinfilm passive components including high volumetric capacitance densities, higher quality factor, and

thinner form-factors are needed. To accomplish these, a new capacitor integration concept based on high surface area electrode-electrode transfer is demonstrated. Fig. 1.6 depicts a schematic cross-section of such nano-porous electrodes on a glass substrate. A novel approach was employed in order to realize the inductors with the required density and quality factors on the backside of the TPV glass substrate (Fig. 1.5). Single-layer RDL-based spiral inductors are modeled, as shown in Fig. 1.7. The RDL based structures are designed to reduce the DC-resistance. This will help reduce the impact on the overall module efficiency.

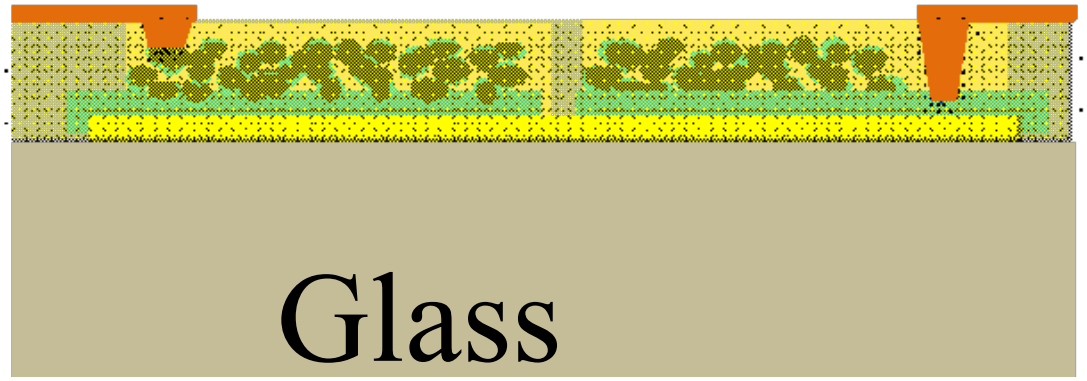


Fig. 1.6: Schematic cross-section of nano-porous electrode on glass substrate.

The 3D IPAC concept is demonstrated through the integration of the building block technologies described above. The research addresses the challenges of high parasitics, sub-par frequency performance and module size, by integrating ultra-high density passives and actives on ultra-thin substrates interconnected by through vias.

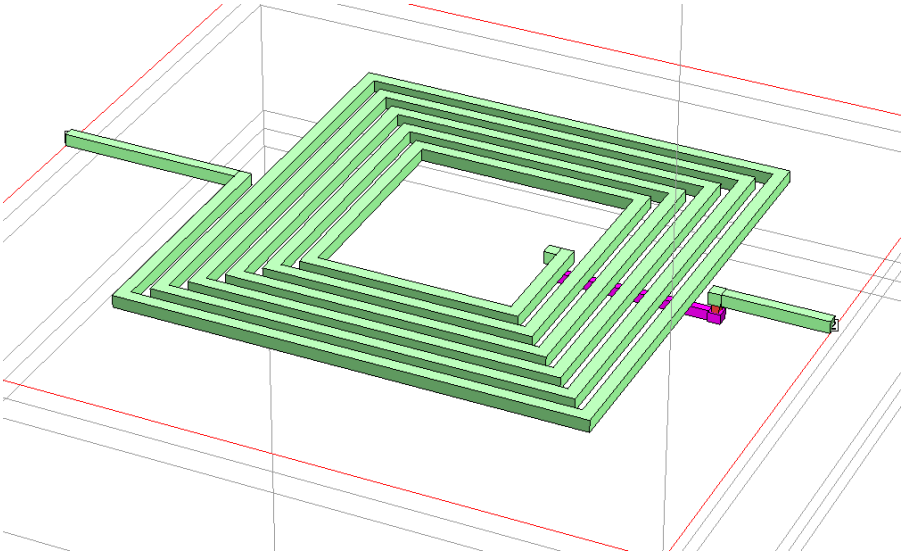


Fig. 1.7: Schematic of an air-core inductor on ultra-thin glass substrates.

1.5 Research Tasks to Address Challenges

1.5.1. Advanced Capacitor Technologies:

1.5.1a High-k thinfilm Capacitors: This task focuses on thinfilm capacitor fabrication using high-k ferroelectric barium strontium titanate (BST) with glass-compatible electrodes. There are two major subtasks.

a. Thinfilm Process Development and Capacitor Fabrication: Fabrication of thinfilm lanthanum nickel oxide to replace copper and nickel. Develop glass-compatible crystallization process for BST.

b. Structural and Electrical Characterization: Structural characterization using SEM (Morphology), XRD (Crystallinity) and XPS (Inter-diffusion) and electrical characterization for leakage current, BDV and capacitance density.

1.5.1b High-surface area capacitors: A novel Si nanowire-based approach is explored to achieve 10-100X enhancement in volumetric capacitance densities compared to trench capacitors. The key research sub-tasks are:

a. Electrical Modeling and Component Design: Develop analytical model to study the frequency response of nanowires with different bulk resistivities.

b. Fabrication of Si Nanowire capacitors: Develop processes to etch polycrystalline Si to achieve low ESR electrodes and form high-density capacitors.

Structural and Electrical Characterization: Structural characterization using SEM and electrical characterization for leakage current, BDV and capacitance density.

1.5.2 Advanced Inductor Technologies:

1.5.2a Electrical Modeling and Component Design*:* Modeling using 2.5D MOM (Method of Moments) and 3D FEM (Finite Element Models) to achieve 80 – 100 nH/mm^2 with Q > 35 @ 100 MHz

1.5.2b Component Fabrication and Characterization*:* Develop a process to fabricate integrated air-core inductors on ultra-thin glass substrates using single-layer RDL to achieve the required metrics. Electrical characterization of the fabricated inductors was performed for inductance density and Q-factor using a Vector Network Analyzer (VNA).

1.5.3. 3D IPAC Power Module: Integrated L and C:

1.5.3a Electrical Modeling and Design: 3D IPAC Package Modeling to extract parasitic R, L and C and optimize via number, size and placement for lowest loop inductance.

1.5.3b Design and Fabrication of complete 3D IPAC power modules with integrated L and C:

High-density thinfilm Capacitors using a foil-transfer approach: Develop foil-transfer process to fabricate integrated high-density Ta capacitors (100 μF/cm^2) on ultra-thin glass using micro-vias and novel adhesives.

Ultra-thin 3D IPAC with integrated L and C: Use the key building block inductor and capacitor integration technologies to fabricate a single ultra-thin 3D IPAC glass based power module.

1.6 Dissertation outline

The outline of the dissertation is listed below and is based on the strategy described in the previous section.

Chapter 2 presents the literature review. The key component technologies required for power supplies are discussed in the first part of the chapter. Dominant packaging technologies currently used for power modules are described next with focus on moderately low-power modules used for mobile processor systems as is the theme of this dissertation.

Chapter 3 presents the first class of advanced capacitor technologies focusing on high-k thinfilm capacitors using barium strontium titanate (BST) as the dielectric. Material and process design is described for both base metal (copper and nickel) and conducting oxide (lanthum nickel oxide) electrode structures. The electrical and structural characterization is presented next.

Chapter 4 presents the second class of advanced capacitor technologies focusing on Si-nanowires as high-surface electrodes for high volumetric density capacitors. Fabrication of the electrode structure using chemical vapor deposition and wet-etch processes is described first, followed by structural and electrical characterization.

Chapter 5 presents inductor and capacitor integration on ultra-thin glass substrates. Electrical modeling and design results are described at the beginning to show the benefits of a 3D integrated approach. A physical design for ultra-thin glass panels is evolved from the modeling. The third part of the chapter defines the fabrication process. The electrical

and structural characterization of the entire 3D integrated inductor and capacitor are shown in the final part of the chapter.

Chapter 6 concludes the work presented in this dissertation and summarizes the key findings and contributions. It also provides suggestions for future work.

CHAPTER 2

LITERATURE REVIEW: POWER MODULES AND COMPONENTS

This chapter describes the evolution and recent advances in low-power modules (1-10 W), widely used in portable and mobile computing applications. Traditionally, such modules are manufactured with discretely-packaged actives and passives that are then assembled on the PWB. Such an approach has three primary limitations for emerging needs. Placement of components on the board far away from the active ICs results in large interconnect lengths with correspondingly large electrical parasitics, which make it difficult to maintain low output impedance over the required frequency range. Another challenge is achieving high converter efficiency. These modules also consume large real estate in both X, Y and Z dimensions with a volume of ~50 mm^3. The trend towards increasing power densities with reduced supply voltages and tighter voltage tolerances is forcing designers to place voltage regulators closer to the active dies. Hence, multiple approaches have been explored to miniaturize the power modules, reduce the parasitics and improve the performance. These approaches are classified in Fig. 2.1 as discrete, embedded discretes, embedded films (package or on-chip), and 3D integrated passives and active components (3D IPAC). This chapter focuses on reviewing these advances. It also describes the key power component technologies, which enable such advances.

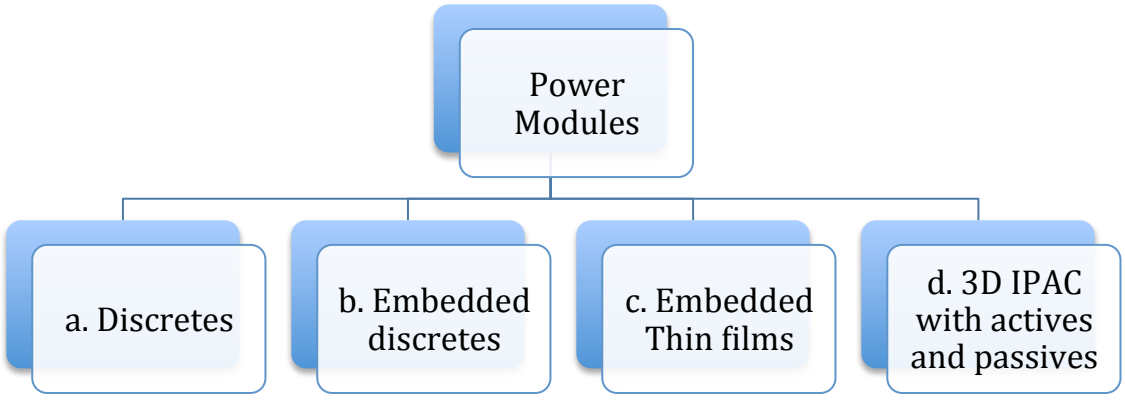


Fig. 2.1: Classification of power modules based on the passive integration approaches.

2.1 Power Modules

2.1.1 Discrete Power Modules:

Power modules are traditionally manufactured by wirebonding dies on leadframe packages. The passive components and other supporting circuitry are mounted as separately-packaged devices on the board, adding to the total real estate. With this approach, the long interconnect lengths and inductive wirebonds degrade the electrical performance because of parasitics. With increasing need to miniaturization and higher power densities, leadframe packaging technology is reaching limits. Many technologies with advanced interconnections are being explored to enhance miniaturization and performance beyond wirebond packages. These include Die dimensional ball grid array (D^2BGA), metal post area technology, BGA MOSFETs and flipchip die attachment for

MCMs. To overcome the size and performance challenges with these 2D approaches, vertical die integration is also evolving. Fig. 2.2 shows one step in that direction with vertical MOSFETs using TIs POWERSTACK^{TM} technology.

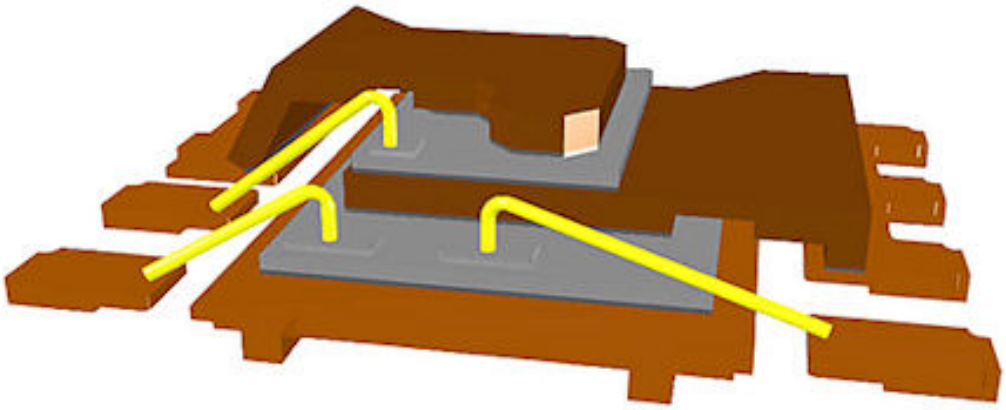


Fig. 2.2: TIs POWERSTACK technology in a leadframe package with wirebonds and Cu clips [10].

Discretes for high-frequency decoupling**:** A steady voltage supply is important for the proper functioning of an IC. High-frequency switching in the active IC can lead to large voltage spikes because of the interconnection parastics. Drastic changes in voltage across the power-supply rails can result in erroneous switching of the transistors. State-of-art discrete voltage regulator modules are only effective for stabilizing voltages up to 1 – 10 MHz switching operations. Decoupling capacitors are used all over the power delivery network to reduce the magnitude of the voltage-spikes and maintain stable power supplies. They are charge reservoirs and act as local power supplies. They help supply

charge when there is a droop in the voltage and absorb it when there is a spike. This levels out the fluctuations and maintain a constant voltage across the power ground planes.

Die-side capacitors are used for low-frequency noise harmonics, and are placed close to the voltage regulator modules (VRMs) on the PCB. High-frequency microprocessor packages like the one from Intel, shown in Fig. 2.3, also have land-side decoupling capacitors on the back of the package. Such land-side decoupling capacitors are used for higher frequencies and are mounted on the package very close to the active IC. These are required to maintain a constant voltage rail across a broadband of frequencies.

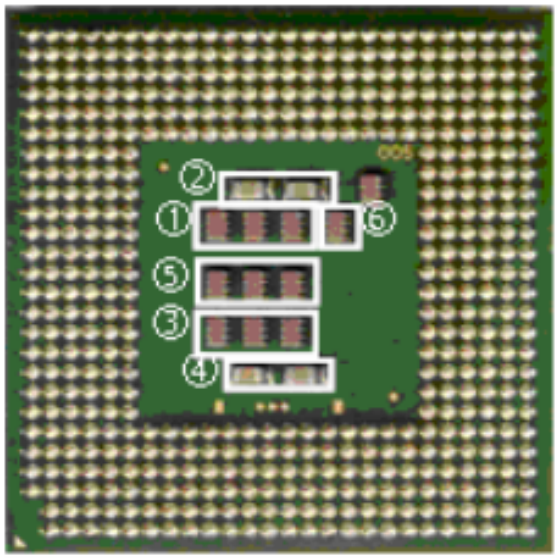


Fig. 2.3: MLCC capacitors mounted on the back of BGA package(Intel) [11]

2.1.2 Modules with embedded discretes:

Several advances were reported in embedded discrete active and passive components in the package to form integrated modules with superior miniaturization and performance. One such approach is TI's MicroSIP power module. The concept involves using an embedded die (~130 μm) in between laminate layers. RDL layer is patterned on the die, prior to embedding, using a semi-additive plating process. The module requires one inductor and two capacitors that are mounted on the top surface. Therefore, the process goes beyond the traditional WLCSP to provide fan-out and 3D routing layers to interconnect the passive components. The 3D interconnects for passives are formed by a combination of mechanically drilled through-vias and laser- ablated micro-vias. The SMD mounted components dominate the height of the MicroSIP module. Fig. 2.4 shows a cross-sectional view of this MicroSIP module [8].

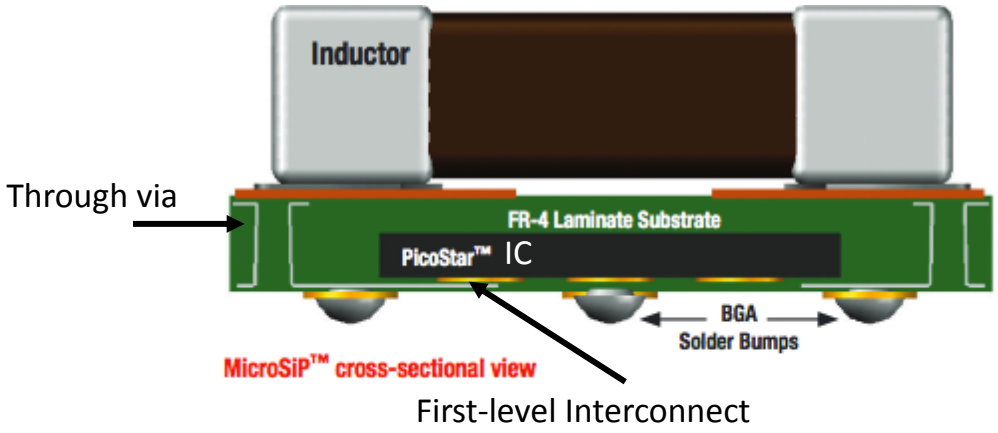


Fig. 2.4: Cross-sectional view of TIs MicroSIP power converter module. [8]

Another such approach is TDK's embedded multi-phase power module. This module can support up to 23 channels with a maximum output current of 2.6 A. It includes a power IC embedded in the substrate using TDKs SESUB technology, which stands for semiconductor embedded in substrate. SESUB allows for embedding ultra-thin 50 μm dies in the substrate. Multiple chips can also be embedded with this approach to help increase functionality. The embedding of the IC helps improve thermal performance and EMI shielding. The thermal performance improvement is because of the IC being in complete contact with the laminate layers with micro-patterned Cu interconnects that help with heat distribution. The SESUB technology boasts of reducing the module size by 45%. The passive components are SMD mounted on the top of the substrate. This results in a module size of 11 x 11 x 1.6 mm^3. Fig. 2.5 shows a SESUB PMU module from TDK. Further miniaturization can be achieved and performance improved with the integration of passive components in the substrate.

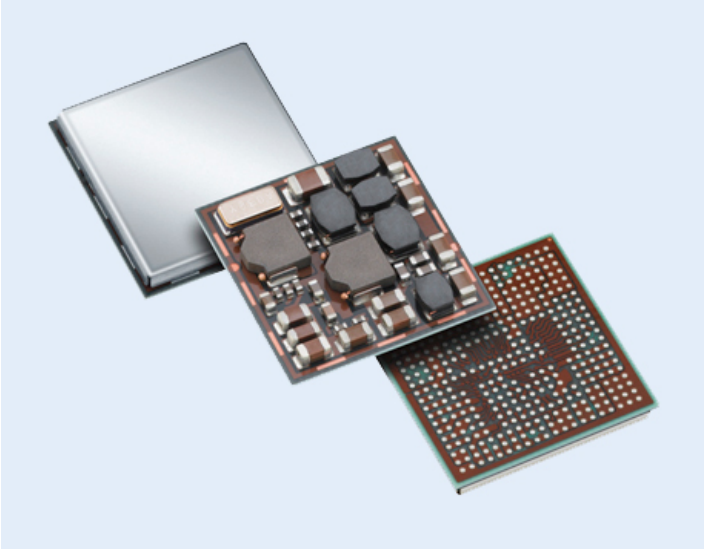


Fig. 2.5: TDKs SESUB PMU modules integrate all essential power converter devices for mobile applications [12].

Murata reported its LXDC inductor series using ferrite-embedded substrate to embed the power inductor, as seen in Fig. 2.6. This approach eliminates the need for surface-mounting the power inductor, which is typically the largest component in a system. With this embedded structure, the ICs can be mounted directly above the power inductor coil with minimal interconnect length and correspondingly low leakage radiation noise. In addition to better EMI noise suppression and a smaller size, up to 3A, can be delivered with input voltages ranging from 2.7-5.5V in a volume of ~50 mm^3 (5.7 x 5.0 x 2.1mm^3).

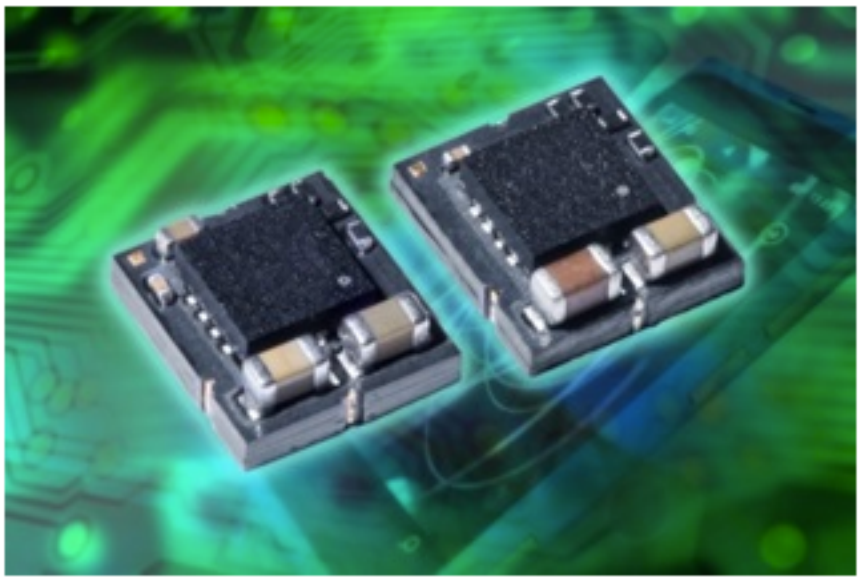


Fig. 2.6: Murata's uDC-DC converters with embedded ferrites [13].

Another approach to improve performance of power modules uses embedded discrete capacitors, as seen in Fig. 2.7. The IC can be mounted on package on top of the capacitor. This allows for shorter interconnect paths resulting in lower parasitics and improved high-frequency performance. Several methods have been explored in embedding of discrete components but have met limited success because they require improvements in

materials, interconnections and substrate technologies for improved reliability. Cost also remains as a major challenge.

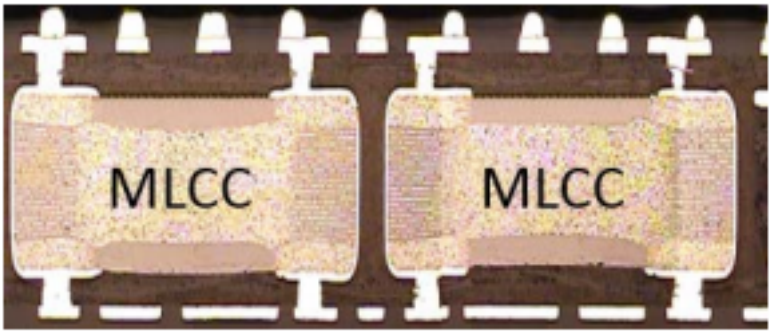


Fig. 2.7: Power module substrate with embedded discrete capacitors[14] .

2.1.3 Power modules with embedded films (On-chip and package embedding):

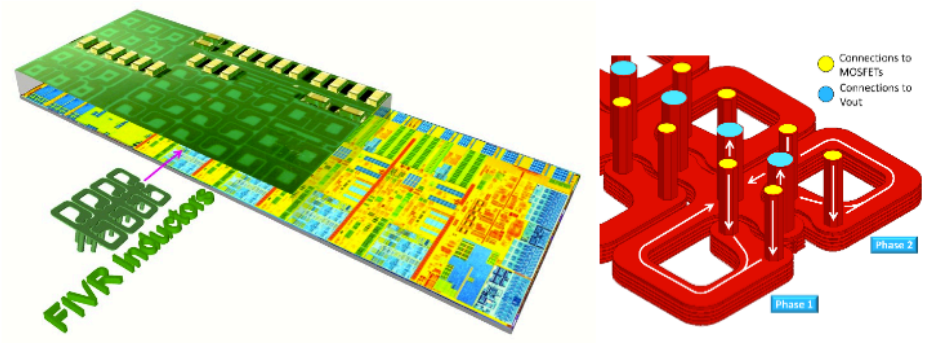
On-chip power modules: The need for fine-grained power management has led to separate power supplies for each of the different microprocessor blocks. Traditionally VRMs are assembled on the board, as described above. Adding a new VRM on the board, for each of the microprocessor functions, increases the overall system size. On-chip voltage regulators address this challenge and also mitigate the challenge of large parasitics due to interconnect lengths. They, thus, provide faster response and improved power delivery. These regulators can be operated at significantly higher frequencies, reducing the size of the power components. However, on-chip converters are known to degrade converter efficiency, increase the process complexity and die cost [15-17].

The most common on-chip regulators are based on switched- capacitor topology. They are gaining a lot of attention because of the ease of their implementation. They are primarily based on embedded trench or (Metal-Insulator-Metal) MIM capacitors on chip, and therefore simpler than traditional converters that use switches with both capacitors and inductors to regulate the voltage. This makes them very attractive for on-chip power conversion, as implementing inductors on-chip is still a very complex and expensive process[18, 19]. Table 2.1 shows a comparison between switched capacitor and inductive converters. The on-chip capacitor technologies are discussed in Section 2.2(c).

Table 2.1: Comparison between switched capacitor and inductive DC-DC converters [20]

	Switched Capacitor	Inductive
Component Technology	• Readily available • Bulk CMOS – low density • MOS Caps – Moderate Density • High A.R. trench – High density	• Very complex process to integrate on-chip
Scalability	• Linear	• Very complex to scale design
Efficiency	• Better at low-power	• Better at high-power
Power range	• Low power < 1.5 W	• Wide range
Power density	• Low power but high power achievable with Trench or SOI	• High Power

To improve performance, achieve increased miniaturization and lower the cost, INTEL introduced the Haswell line of processors with fully-integrated voltage regulators (FIVRs) as described by Lambert et.al. They consist of the power MOSFETs and control circuitry implemented on the microcontroller. The capacitors are formed using a MIM capacitor on-die or with trench capacitors. The air-core inductor layers are fabricated on the bottom layers of the BGA package. Inductance values of 2 – 10 nH are achieved using this process. These low values are attributed to the use of a non-magnetic (polymer) core. Such a process allows designers to precisely select and place components at the desired locations. Fig. 2.8 shows the FIVR with and enlarged view of the FIVR inductors side-by-side.



(a.)

(b.)

Fig. 2.8: (a.) Back-side of Intel's Haswell processor with FIVR and (b.) enlarged 3D view of FIVR inductors [21].

2.1.4 3D IPAC Functional modules:

As a next step in the evolution of integrated and miniaturized functional modules, GT-PRC proposed an innovative 3D IPAC concept, described in Chapter 1. The 3D IPAC concept achieves enhanced miniaturization and, performance enabled by ultra-short interconnections between actives on one side and passives on the side in an ultra-low loss glass medium. . This technology was recently demonstrated with 3D integrated inductors and capacitors for RF applications. Spiral inductors were designed with values up to ~ 20 nH and capacitors of 12 – 15 pF were obtained using this method. These components are integrated on ultra-thin glass substrates with through vias using a four-metal layer RDL process [22, 23]. This approach allows for integration of components on either side of the ultra-thin substrates interconnected by ultra-short vertical interconnections, leading to ultra-miniaturized multi-functional systems. Such an approach is expected to be a very

low cost as well since the 3D IPAC substrate is fabricated from very large panels of 150 mm or larger [4, 24-28].

2.2 Power Components

Typical power regulator modules consist of an active IC along with an input decoupling capacitor, a storage inductor and an output filter capacitors. The lack of critical storage components such as capacitors and inductors with the required volumetric densities and form-factors to handle high power densities at high efficiency continues to pose a major challenge in power supplies. Discrete components, in spite of their dramatic size reduction and performance improvement during the past two decades, face major bottlenecks because of the need to be thinner than 150 microns, complexity in pick-and-place such ultrathin components that are less than 100 microns[29]. This led to dramatic shift from discretes to ultrathin IPDs, embedded passives and onto on-chip passives as shown in Fig. 2.9. This section describes these advances [30].

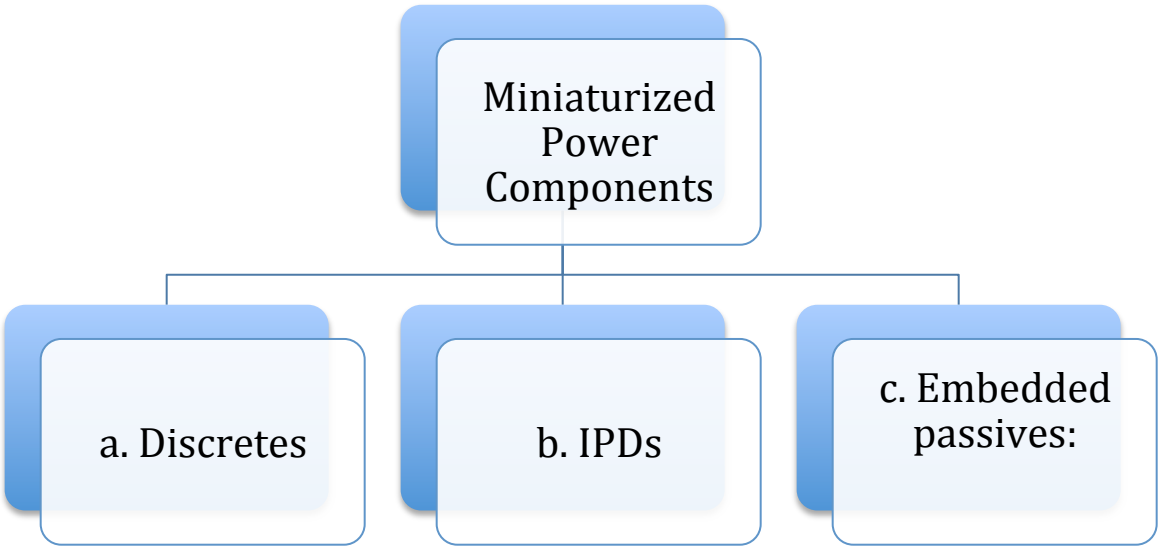


Fig. 2.9: Classification of power components.

2.2.1 Advances in Discrete components:

Discrete components are dominated by aluminum, multilayered ceramic and tantalum capacitors. These are reviewed in this section.

1. Aluminum Capacitors:

   Aluminum capacitors are formed using etched Al foils as the anode and an electrolyte (solid or liquid) as the cathode, separated by a thin oxide layer. Fig. 2.10 shows a cross-section of an Al capacitor. The oxide layer is formed with anodization process. These devices have polar characteristics because of the anodization process.

State-of-art SMD Al capacitors have capacitance values that range from a few nF up to a few mF with voltages ranging from < 5V to > 500V. The sizes varying from 0201 SMDs to capacitors with case sizes greater than 100 mm. Aluminum capacitors are available with both liquid and solid electrolyte. For most power delivery applications in mobile systems, solid electrolyte capacitors are the primary choice as they are readily available in SMD form-factors. Currently most research and development works focuses on lowering ESL and ESR while trying to improve capacitance density at a higher operating temperature. The ability to deliver these properties in SMD configurations with relatively low-cost is a primary area of interest.

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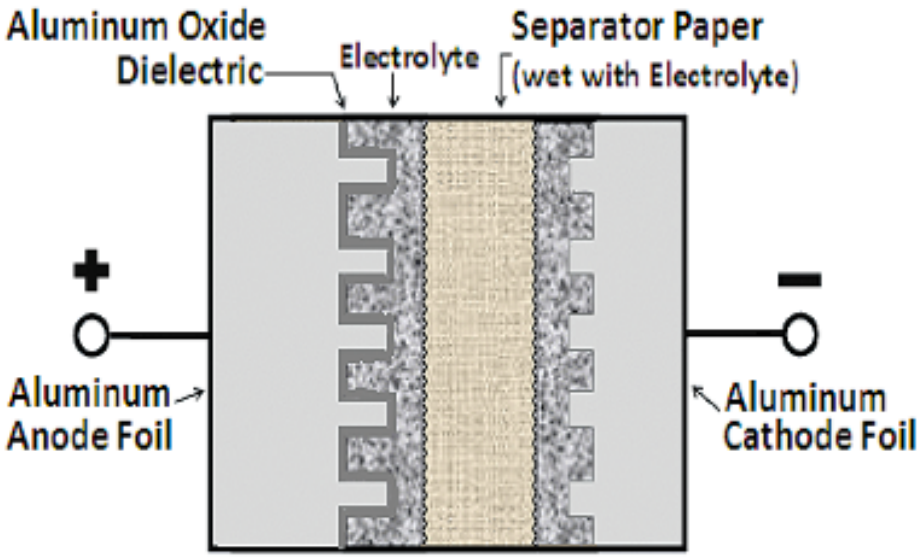


Fig. 2.10: Aluminum capacitor cross-section [31].

The volumetric capacitance density of Al capacitors has continually increased over the past few years. However, as the etching capacity of Al is reaching its

physical limits further increase in capacitance density has become a major challenge. This has led to the exploration of newer and alternate methods for increasing capacitance density, which include vapor deposition and alternative cathode processes such as Ti coated Al.

Aluminum capacitors are being considered as replacements for Ta capacitors. Al capacitors with solid electrolytes have very low ESR and ESL and are very attractive for decoupling circuits. However, they cannot match the volumetric efficiency of tantalum capacitors. Another drawback is the high frequency roll-off. Aluminum capacitors are known to show roll-off starting at 100s of kHz. Hence, even with the advantages in lower ESL and ESR, this turns out be a major deterrent for decoupling applications that require frequencies above 10s of MHz and in some cases even GHz.

Al capacitors have found widely in the automobile and industrial applications. SMD capacitors, which can withstand harsh conditions, such as high temperature and pressure currently in major demand. These capacitors require several advances in packaging technologies.

2. Tantalum Capacitors:

Tantalum forms a polar, electrolytic capacitor. A sintering process is used to form a high surface area electrode starting from a Ta powder. The oxide dielectric is conformally formed on the sintered tantalum particle using an anodization

process. The oxidized Ta is then coated with a cathode. MnO_2 and conducting polymers are the most popular cathodes. Ta capacitors are used in several applications some of which include bypass and decoupling. These capacitors are highly reliable and are used for industrial, automobile and military applications.

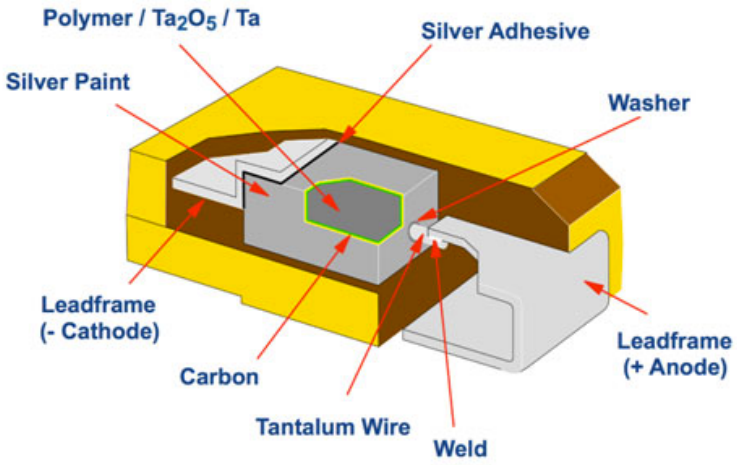


Fig. 2.11: Ta capacitor construction [32].

Fig. 2.11 shows the construction of a Ta capacitor. The processing begins with the sintering of Ta powder around a wire. The powder is usually coated with organics for improved distribution. The particle shape and size define the final volumetric density. Sintering is used to form a good electrical and physical contact between the particles. This process usually involves heating the Ta powder in a vacuum oven at highly elevated temperatures. The heating also helps to burn away the organics.

After sintering, an anodization process is used to create Ta_2O_5 and then a cathode is dispensed to complete the capacitor structure. Manganese oxide or conducting

polymers are used as cathodes because of their self-healing characteristics. Self-healing improves reliability over time by local isolation of the defects from the conducting path[33, 34]. However, the ESR achieved from self-healing cathodes is relatively high. This results in capacitance droop with frequency.

Hence, conducting polymers with better conductivity were developed as alternative traditional cathode materials. The major advantages of conducting polymer over MnO_2 are lower ESR, surge robustness and non-ignition failure. Earlier, they were not very popular because of the relatively high cost, higher leakage, low temperature capability and low voltage range. However, over the past few years, conducting polymers have become the primary choice as cathode material for Ta- based capacitors. Advances in polymer chemistries and processes now allow for multiple reflows. As such capacitors are also available that can survive temperatures higher than 125 C.

Tantalum capacitors have the highest volumetric density among all other materials. These capacitors are highly reliable and stable at high temperatures and bias conditions. Ta forms a paraelectric oxide, which means that the capacitance does not drastically change with applied bias. A lot of research work is currently on-going that focuses on improving ESL and ESR characteristics along with improved leakage currents at higher operating temperatures (> 150 C). The one major drawback of these capacitors is that they are polar devices and hence, are required to be assembled with the correct orientation.

For higher volumetric density, Chakraborti et al. have looked at particle sizes lower than 80 nm to achieve capacitance densities beyond 400 μF/cm^2. The major challenge with smaller powders is their sensitivity to sintering and anodizing conditions. The necks formed during sintering are seen to disappear during anodization if high voltages are used. This effect is seen because the oxide layer forms not only around the neck but also through it, resulting in a loss of contact between the pellets. This results in lower capacitance density than is desired.

Ta capacitors are currently available as SMDs with operating voltages from < 5V to > 60 V with a capacitance range of a few nano farads almost up to a mF. The smallest Ta capacitors are available in 0201 configerations but are limited in density (0.01 μF) and voltage of about 4V. Ta capacitors are currently limited to a few 100 kHz. They have a temperature stability of 150 C. The improvement in ESR, ESL will lead to improved frequency performance, leading to more applications.

3. Multi-Layered Ceramic Capacitors (MLCC):

MLCC stand for Multi-layer ceramic capacitors. They are made up of multiple, alternating metal-insulator-metal stacks. Alternative metal layers are connected together to form a common electrode. MLCCs utilize high-permittivity dielectrics such as barium strontium titanate and barium titanate. Fig. 2.12 shows a cross-section of a typical MLCC. These capacitors are not polarized and hence can be connected with either terminal acting as anode and cathode.

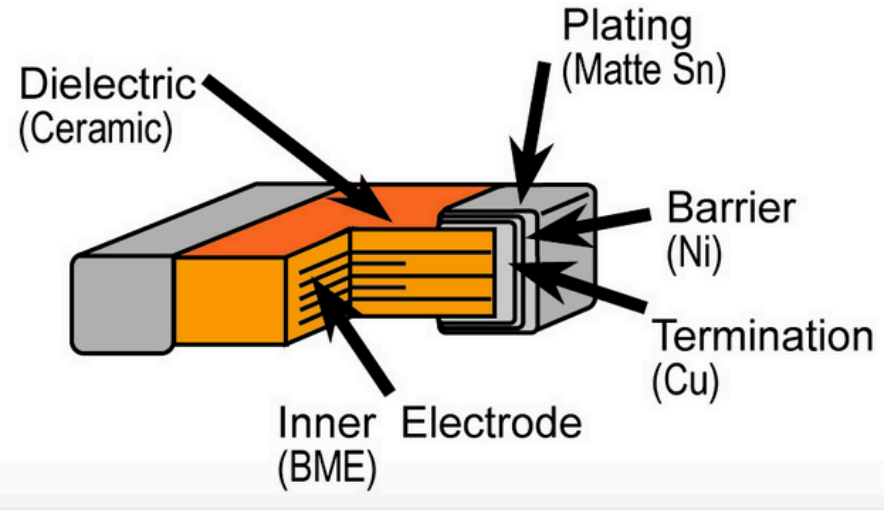


Fig. 2.12: Cross-section showing typical MLCC construction [35]

Traditionally MLCCs were limited in capacitance density and operating voltage range. Therefore, Ta and Al capacitors were used for applications that required higher voltages and capacitance. However, recent advances have resulted in MLCCs with higher capacitance densities and operating voltages. This is mainly because of the improvements in the volumetric density of ceramic capacitors.

The main challenges associated with improving capacitance densities of MLCCs include the use of thinner electrodes and thinner dielectrics. Such advances, however, result in challenges relating to reliability, temperature and voltage stability. Most advances in achieving higher capacitance density have been with reducing the dielectric film thickness and increasing the number of layers. Ultra-thin dielectric layers, however, result in reduction in the maximum voltage rating from 16V to 4V.

There has been a recent trend in moving to base-metal (Ni) electrode systems in place of precious metal electrodes used in traditional MLCCs. Even though there have been major concerns with the reliability of Ni electrodes, they have proven to be a better choice with respect to thermal shock compared to Pt, Pd or Pd/Ag. This is because of the lower CTE mismatch between the metal-dielectric stack when using Ni. The base-metal electrodes also have improved dielectric-electrode bonding over precious metals. This is because of the interfacial reactions between the Ni electrode and barium titanate (BT) during the co-firing process. The high-temperature annealing process required for crystallization of the BT dielectric results in oxidation at the interface leading to improved bonding.

The introduction of Ni electrodes raises one major concern, which is related to oxygen migration to the cathode. When an electric field is applied across the capacitor, the oxygen vacancies migrate towards the cathode reacting with it to form a semiconducting interface. Such an interface behaves like a Schottky barrier. This barrier has a lower insulating resistance compared to pure unreacted metal-dielectric interfaces. This results in lower breakdown voltage and higher leakage currents.

MLCCs show large deviation in capacitance with change in temperature. This challenge has been partially mitigated by introducing dopants into the dielectric. The X5R and X7R dielectrics have much better performance compared to

standard barium titantate. These advances to form more stable dielectrics have helped reduce the size of the capacitors while maintaining high volumetric density.

The need for smaller components that can lead to ultra-miniaturized systems has pushed capacitor manufacturers to build smaller components than ever before. Current state-of-art in smart phones are 0201 and 01005 devices but Murata, which is one of the leading manufacturers of MLCC capacitors, has rolled out a line of 008004 (0.25x0.125 mm^2) devices. However, although these capacitors help restrict the footprint, they are limited in the total capacitance. Typical values range from 1 pF to 10 nF with a rated voltage of 6.3 V [36]. Fig. 2.13 shows the trend of size reduction in ceramic capacitors.

Fig. 2.13: Trend to size reduction in ceramic capacitors [36].

4. Discrete Inductors:

Discrete inductors used in power-supply applications predominantly have a ferrite core with Cu- wire wound around it. Resin with fillers for EMI isolation is used to cover the inductors to provide higher reliability and keep the magnetic field bound to the inductor area. Fig. 2.14 shows a typical construction of an inductor.

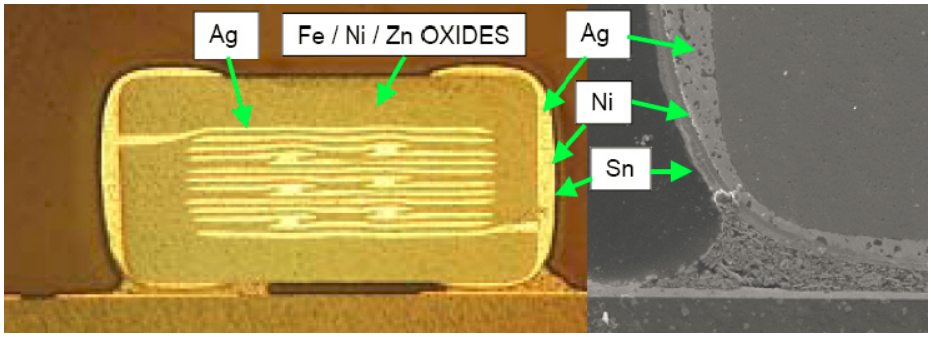


Fig. 2.14: Cross-section of a typical inductor[37].

Inductors are the largest components in power supply modules and form the single major bottleneck for module miniaturization. The increase in inductance is a consequence of increasing the number of layers and increasing the coil windings. This has led to an increase in densities from 870 nH/mm3 to 1850 nH/mm3. This means using thinner layers and tighter lines that increase the ESR. This is highly undesirable as it means higher losses and lower efficiency. Inductors are reaching fundamental limits in their volumetric density, and therefore, alternative solutions for inductor integration are now widely investigated.

Discrete inductors (also referred to as chip inductors) form primary components for most discrete power supplies. They are used for filtering, impedance matching and as chokes. Miniaturization of inductors is becoming extremely important to support increased system miniaturization. Fig. 2.15 shows discrete power module from TI (formerly National Semiconductor)[38] and Fig. 2.16 shows a SiP module also manufactured by TI. Both the modules have discretely mounted SMD capacitors and inductors.

Fig. 2.15: Modular design with discrete components [38]

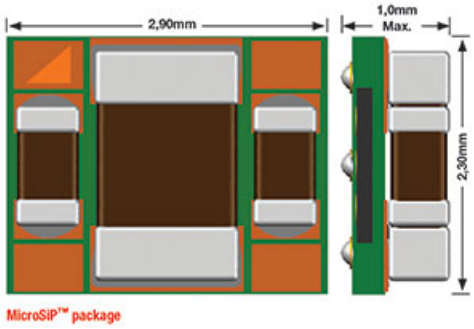
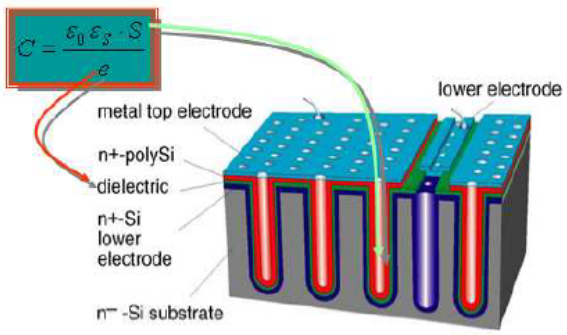


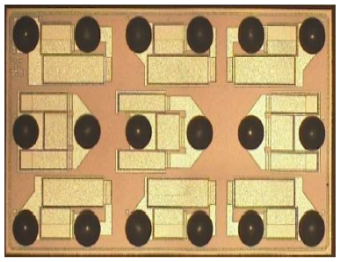
Fig. 2.16: TI's microSIP module with SMD inductor and capacitors [4].

2.2.2 Integrated Passive Devices (IPDs):

Passive components such as inductors, capacitors and resistors fabricated on organic or inorganic substrates using standard package and IC processes such as lithography, sputtering, plating etc are defined as Integrated Passive Devices (IPDs). Silicon-based IPDs usually comprise of trench capacitors. The leading-edge IPDs from IPDiA have trench capacitors with 1 $\mu F/mm^2$ density. Fig. 2.17a shows a schematic of trench capacitor fabrication and 2.17b demonstrates trench capacitors fabricated in the Si substrate. This technology is also being used to fabricate integrated inductors and resistors on passive Si substrates [39].



(a.)



(b.)

Fig. 2.17: (a.) Typical Si trench capacitor construction and (b.) Trench capacitors formed on passive Si substrates [39].

2.2.3 Embedded Passives (Package or on-chip):

The limitations of discrete component technologies have led to the evolution of embedded passives as shown in Fig. 2.9b, where the passives are formed as thinfilms during the package or IC fabrication.

1. Package-embedded capacitors: Package-embedded high-k thinfilm capacitors can have a dramatic impact on system miniaturization by replacing all the surface-mount decoupling capacitors on the board. The evolution of ultrathin high-permittivity dielectrics and nanostructured electrodes enable this trend by providing high volumetric capacitance densities without degrading the electrode resistance and dielectric leakage. This section briefly reviews the advances in high-permittivity (k) thinfilm embedded capacitors.

High-k thinfilm capacitors use 100-1000 nm thick perovskites such as $BaTiO_3$, $(BaSr)TiO_3$, and $Pb(ZrTi)O_3$ as the insulator [40-45]. Fujitsu has reported integration of high-k thinfilms partially crystallized at organic package-compatible temperatures, as shown in Fig. 2.18 [46]. Shinko demonstrated thinfilms integrated on Si interposers with Pt electrodes, with a capacitance density of 2 $\mu F/cm^2$ [47]. A top view of a thinfilm capacitor on Si interposer is shown in Fig. 2.19.

Conducting metal-oxide electrodes are more suitable alternatives to metal electrodes because they enable better electrical reliability at lower cost. They also suppress interfacial reactions, and act as sinks for the entrapment of defects. Wang et.al, have demonstrated capacitors with lanthanum nickel oxide electrodes and lead zirconate

titanate dielectrics using solgel approach. Capacitance densities of above 3 μF/cm^2 and leakage currents of the order of a few μA/μF have been reported.

Several efforts have focused on reducing the crystallization temperature using a hydrothermal process, or by using a foil-transfer process with pre-crystallized films. To obtain high-quality barium titanate films on organic substrates, barium titanate films were deposited and pre-crystallized on freestanding copper films. Fig. 2.20 shows SEM images of high-k barium titanate thinfilms formed with both hydrothermal and solgel processes.

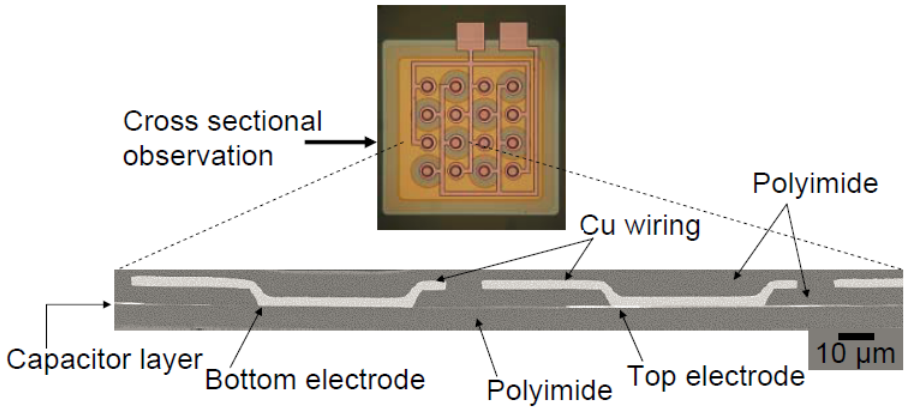


Fig. 2.18: Thinfilm capacitors on organic substrates by Fujitsu[46]

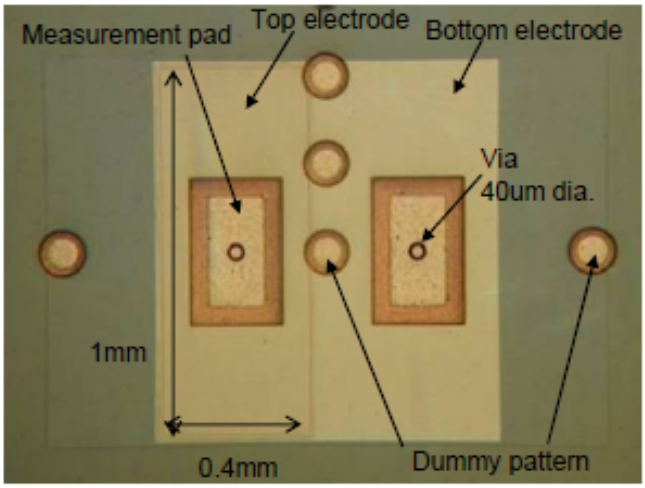
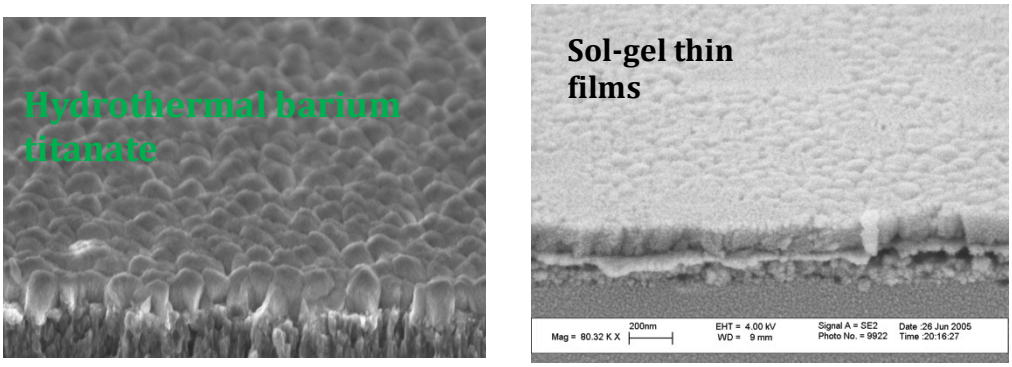


Fig. 2.19: Integrated high-k thinfilm capacitor in Si interposers by Shinko [47]



(a) (b)

Fig. 2.20: Hydrothermal(a) and Solgel(b) barium titanate thinfilms for package-embedding by GT-PRC[40, 45]

2. On-chip capacitors: Passives that are fabricated as part of the active ICs are defined as on-chip passives. Various approaches have been used to integrate capacitors on-chip for various high-speed decoupling applications. One such approach is polysilicon-insulator-polysilicon (PIP) where silicon dioxide is used as the insulator. The silicon is also etched to form deep trenches for higher surface area. Fig. 2.21 shows trench capacitors formed on chip. Another approach uses a metal-insulator-metal stack to form the capacitor. The

most common insulator is silicon dioxide but others such as ALD alumina and hafnia have been explored as alternatives to increase the capacitance density. Fig. 2.22 shows trench capacitors with alumina as the dielectric. Other architectures include woven and vertical parallel-plate capacitors. These too are actively used for on-chip decoupling. Table 2.2 shows a comparison of on-chip decoupling capacitor technologies.

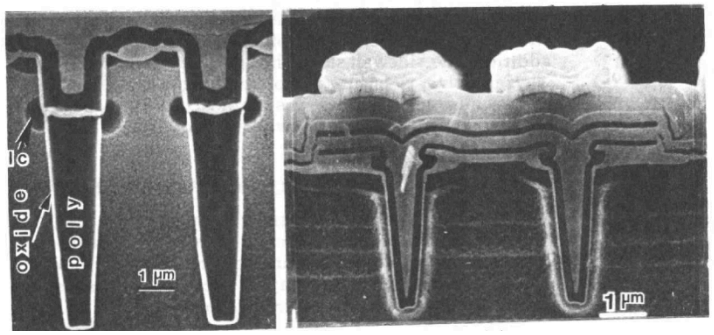
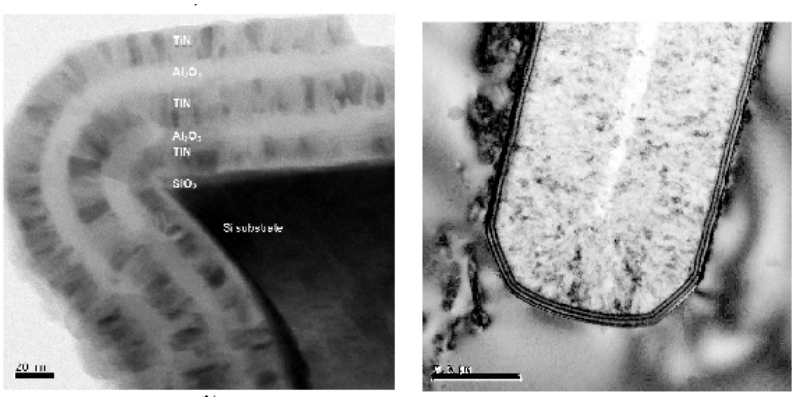


Fig. 2.21: Trench capacitors fabricated in the 1980s for DRAM applications [48]



(a.) (b.)

Fig. 2.22: (a.) SEM image showing trench capacitors in Si formed with Alumina as a dielectric and (b.) TEM image showing various layers of the capacitor [49].

Table 2.2: Four common types of on-chip decoupling capacitor technologies in 90-nm CMOS technology [50]

Feature	PIP capacitor	MOS capacitor	MIM capacitor	Lateral °ux capacitor
Capacitance density (fF/¹ m²)	1–5	10–20	1–30	10–20
Bottom plate capacitance (%)	5–10	20–30	2–5	1–5
Linearity (ppm/volt)	50–150	300–500	10–50	50–100
Quality factor	5–15	1–10	50–150	10–50
Parasitic resistance (m)	500–2000	1000–10000	50–250	100–500
Leakage current (A/cm²)	$10^{i\ 10}$–$10^{i\ 9}$	$10^{i\ 2}$–$10^{i\ 1}$	$10^{i\ 9}$–$10^{i\ 8}$	$10^{i\ 10}$–$10^{i\ 9}$
Temperature dependence (ppm/±C)	150–250	300–500	50–100	50–100
Process complexity	Extra steps	Standard	Standard	Standard

3. Package-embedded inductors**:** Another key bottleneck for miniaturizing power modules is high-density inductors. Traditional inductor SMDs are 0.3-0.5 mm thick, increasing the overall module thickness. This requires the module to be mounted on the board, limiting the overall operating frequency to a few MHz. The need for ultrathin power modules will shrink the inductor size from 300 and to less than 50 microns. This is achieved with package-embedded inductors. Intel's line of Haswell processors employ integrated package air-core inductors along with integrated capacitors to enhance performance and provide increased miniaturization as seen in Fig. 2.23. The required inductance inversely varies with the switching frequency. Increase in switching frequencies is, therefore, more critical for inductor miniaturization. Nanomagnetic films with ultrahigh permeability, frequency stability and low loss are expected to further reduce the component thickness to less than 10 microns [6, 51, 52].

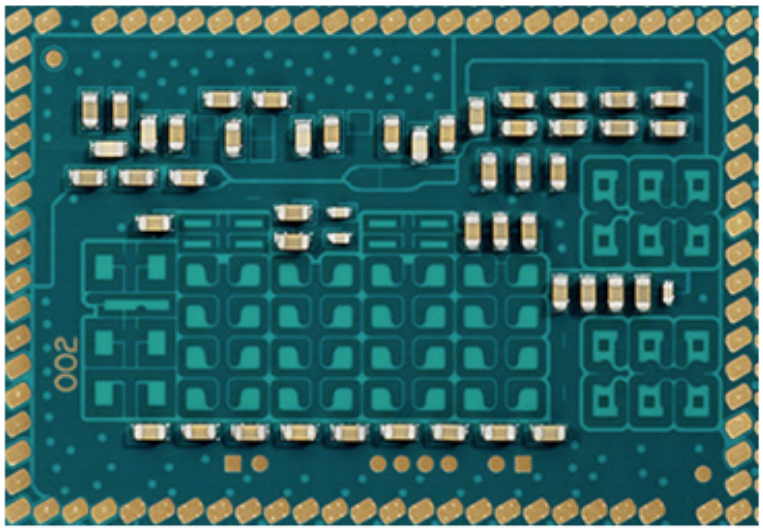


Fig. 2.23: LGA Package embedded air-core inductors for Intel's Haswell processor[6].

4. On-chip inductors: There is an increasing trend towards on-chip integrated inductor solutions for power delivery because of their improved performance and miniaturization. On-chip spiral inductors achieve 10s of nH but occupy valuable large real-estate on the active Si which could otherwise be used for transistors. The use of on-chip magnetics can increase inductance densities, improve quality factors and reduce the required capacitance, leading to improved performance. Limited increase in inductance density has been demonstrated through the use of single layer magnetic materials. By wrapping the magnetic films around the spiral coils using two layers and magnetic vias, Don Gardner et al. have demonstrated a 19X improvement in inductance and a 16X improvement in Q-factor. Fig. 2.24 shows an inductor-fabricated on-chip using a CoZrTa. However, these films do not have sufficient volume to handle high power.

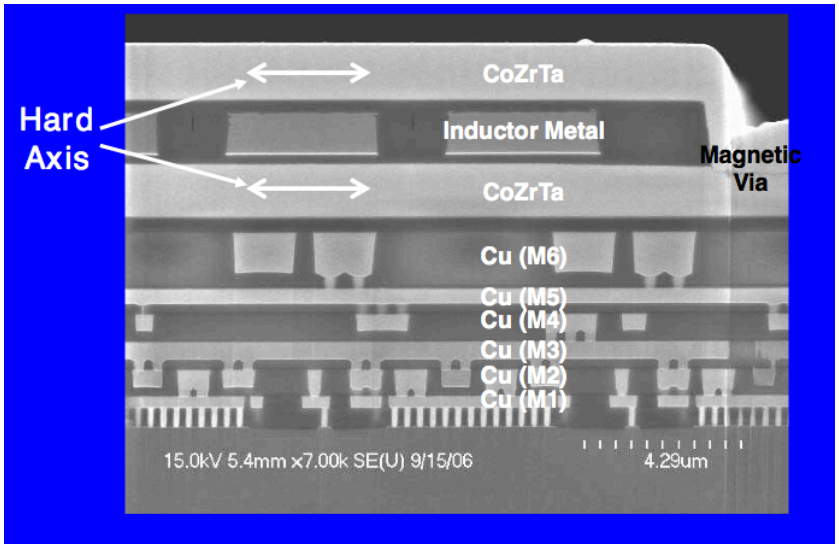


Fig. 2.24: Inductors fabricated on-die using 130 nm process [53]

2.3 Summary

The key integration approaches for low-power modules are described in the first part of the chapter. These approaches range from modules with SMD passives to embedded and on-chip passives. The performance and size benefits with embedded passives are highlighted. The second part of the chapter described the key classes of power-supply passives.

CHAPTER 3

HIGH-K THINFILM CAPACITORS

3.1 Introduction:

This chapter describes demonstration of glass-compatible thinfilm capacitors for power-supply noise filters, (or decoupling capacitors) using conducting oxide electrodes as a superior alternative to conventional metal electrodes. Such capacitors are traditionally integrated through surface-mount devices (SMDs). Integrated capacitors as thinfilms can lower power supply noise and improve power integrity, particularly if these capacitors can achieve high capacitance densities and are very close to the switching transistors. These benefits can be achieved with an unique approach that involves high-permittivity thinfilm dielectrics directly deposited on 3D IPAC-like glass substrate architecture to enable ultra-short interconnection distances between the capacitor and the active chip, [54, 55]. This chapter focuses on exploring, developing and demonstrating such thinfilm capacitor processes on glass substrates.

3.2 Background – Integration of Thinfilm Capacitors with High-Permittivity Dielectrics

Thinfilm decoupling capacitors in packages have been achieved with polymers or polymer composite dielectrics oras paraelectric oxides on silicon substrates [56-58] because of their ease of process integration. These are, however, limited to capacitance densities of ~0.1—5 nF/mm^2. Thinfilm capacitors with high-permittivity dielectrics, on the other hand offer densities of 20-50 nF/mm^2, and are more desirable for power supply. However, they face several challenges in integrating them as thinfilms directly on

substrates. This section reviews the state of the art in high-permittivity dielectrics and their process integration to form high-density capacitors.

High-Permittivity Dielectrics: Dielectrics with permittivity of above 100 are referred to as high-permittivity dielectrics. Unlike polymers or binary oxides that show low polarizability from electronic or ionic polarization, high-permittivity dielectrics undergo large cationic displacement under electric fields, leading to much higher polarizability. Under certain conditions, these materials can also undergo spontaneous polarization by forming domains, which then reorient in the direction of electric field to give much higher permittivities. These materials are referred to as ferroelectrics.

Ferroelectric ceramics are most commonly based on the perovskite crystal structure. Fig. 3.1 shows a representative crystal structure with A being the large cation, B being the smaller cation and O being the oxygen atoms. The larger cations are located at the corner, the smaller cations form the body center and the oxygen ions are present at the face center [59].

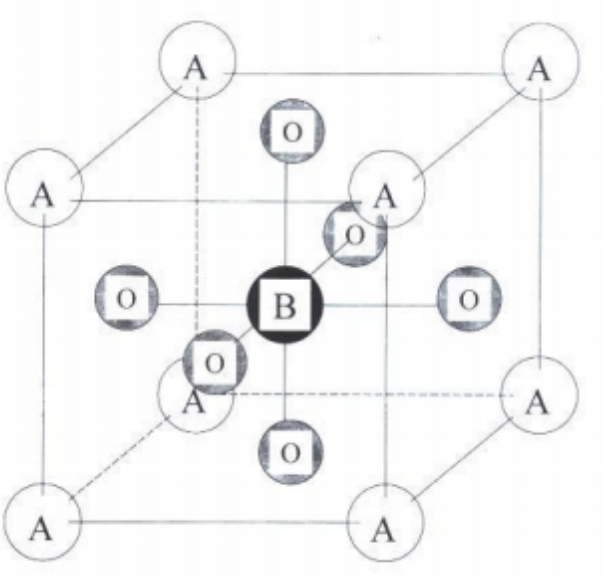


Fig. 3.1 Ferroelectric ceramics showing perovskite crystal structure [59].

Ferroelectrics transform into paraelectrics beyond a certain temperature called the Curie temperature, Tc. At this phase-change temperature, highest dielectric constant is achieved. Ferroelectrics below Curie temperature have a positive temperature coefficient of capacitance. Beyond Curie temperature though, in the paraelectric phase, these materials have a negative TCC [60].

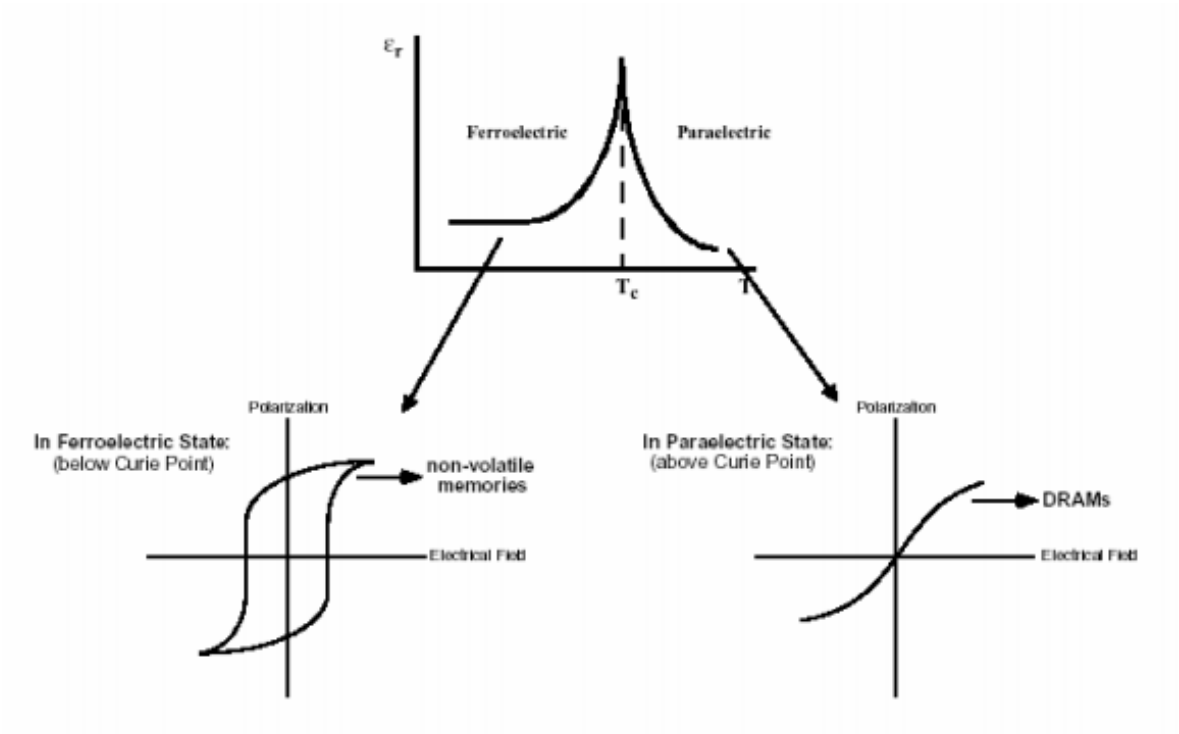


Fig. 3.2: Phase transitions in ferroelectrics and the associated polarization characteristics [60].

The dielectric constant follows a Curie-Weiss in the paraelectric phase [60]. In the ferroelectric phase, a strong hysteresis behavior is observed making, them suitable for non-volatile memory applications, whereas in the paraelectric phase they lose their spontaneous polarization. These polarization characteristics are shown in Fig. 3.2. In the

paraelectric phase, the hysteresis behavior is absent, making them very attractive for DRAM applications. Because of their high permittivity in both phases, they are widely used for capacitor applications. Materials such as lead titanate, lead zirconate titanate and lead lanthanum zirconate titanate have also been explored as piezoelectric for MEMS applications.

$$\epsilon_r = \frac{C}{T - T_c} \tag{3.1}$$

Barium Titanate is the most widely used ferroelectric in multi-layered ceramic capacitors (MLCC) capacitors today. The BT structure is cubic and is similar to one seen in Fig. 3.1. The larger cations (A) are Barium, the smaller cations (B) are Ti, and the O represents the oxygen atoms. In the case of BST, the larger cations can be either barium or strontium. BST undergoes phase transition at Curie temperature similar to other ferroelectrics. The addition of strontium results in a shift in Curie temperature. The Curie temperature is known to reduce with an increase in Sr^+ content [61, 62] [63].

Ferroelectrics have different properties in the bulk form versus thinfilms. The bulk material is known to have a sharp peak at the Curie temperature. The dielectric constant at this temperature is known to be upwards of 10,000. However, the dielectric constant is found to be much lower in thinfilms. The temperature dependence is also found to be much lower with thinfilms. Fig. 3.3 shows the effect of temperature on bulk BST versus thinfilm BST.

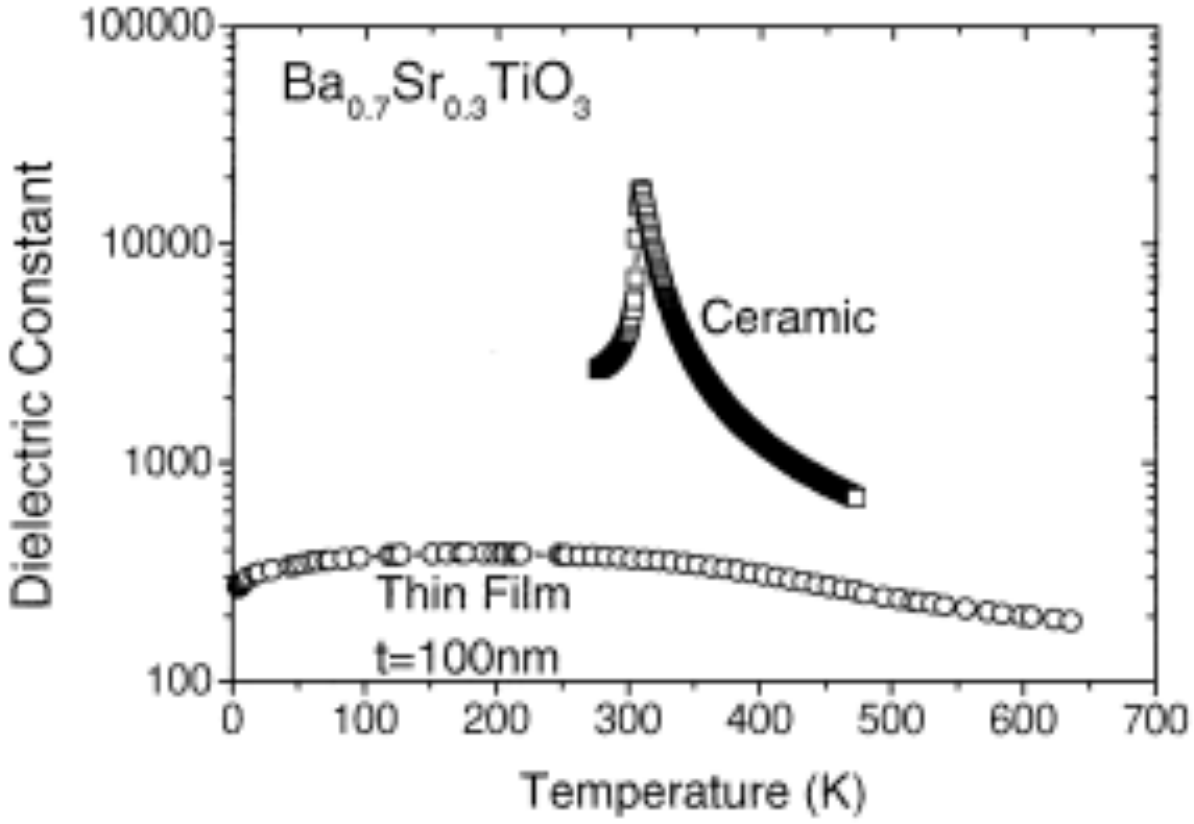


Fig. 3.3: Temperature dependence of BST bulk material and thinfilms [64].

Integration of high-K dielectrics in packages: Barium strontium titanate (BST) and barium titanate (BT) with high permittivities of 200-500 are most preferred candidates as ferroelectric thinfilm capacitors. They have no major toxicity concerns that are associated with lead-based perovskites such as lead zirconate titanate (PZT). The electrical properties, defect density and long-term reliability of sputtered BST films depend on sputtering power, chamber pressure, BST composition, post-annealing process and the bottom electrode system [65, 66]. However, these high-permittivity thinfilm dielectrics have not been successful because of the processing challenges associated with crystallizing such films at high temperatures of around 700 ^{o}C.

Several efforts have focused on reducing this crystallization temperature or by addressing the process-compatibility issues using a foil-transfer process. Advanced high dielectric constant thin-film capacitors using low-temperature (<100 C), organic-compatible processes have been developed using hydrothermal crystallization route. As an alternative approach to obtain high-quality barium titanate films on organic substrates, barium titanate films were deposited on free-standing copper films and heat-treated at high temperatures with the copper films as the base. These ceramic film-coated copper foils were then integrated into organic packages using a foil-transfer or foil-lamination processes.

High-permittivity thinfilm capacitors on silicon have been primarily investigated using Pt electrodes with titanium, or tantalum as the diffusion barriers and adhesion promoters between Pt and Si. However, several challenges such as long-term electrical fatigue which results in effective loss in polarization due to cyclic voltage switching over time, inadequate adhesion, and high costs have driven researchers to find alternative electrode systems such as copper or nickel [67]. Because of their relatively low melting points, Cu or Ni metal electrodes, however, undergo recrystallization and grain growth during the heat treatment at temperatures as low as 450 C, resulting in rough metal-oxide interfaces [68]. In addition, these electrodes are more prone to oxidation during the dielectric crystallization processes resulting in diffusion into the dielectrics or substrates [69]. This leads to microcracks and voids, which result in high current leakages, low BDV and low process yields. It is, therefore, important to identify and study suitable diffusion barriers between the electrodes, dielectrics and substrates, and optimize the post-annealing processes to minimize these detrimental interfacial reactions to improve the overall capacitor performance.

Various barriers were reported to address the electrode instabilities with copper and nickel electrodes. On the silicon side, a double-barrier of Ta/TaN was found to be effective in suppressing the copper diffusion [70]. Alternatively, an alloy of Cu-Mn was also found to suppress copper migration as the Mn migrates first into the silicon interface to form thin barrier oxides [71]. TiAl has been explored as a barrier at the Cu/dielectric interfaces, to prevent interfacial reactions. In most of these approaches, a thin interfacial reaction layer, which acts as an additional dielectric layer, forms between the metal and BST [68]. This interfacial layer dilutes the overall capacitance density of the dielectric films.

Conducting metal-oxide electrodes such as lanthanum nickel oxide are most suitable replacements for Cu and Ni metal electrodes because of their stability in high-temperature and oxygen atmospheres. They also suppress the interfacial reactions, and act as sinks for the entrapment of defects [45, 72]. LNO forms a perovskite oxide electrode that goes one step beyond by providing a lattice-matched structure with the perovskite dielectrics thus minimizing the CTE mismatch. Hence, they are more ideally-suited for enhancing the reliability of the dielectrics by remaining stable at the high (>600 C) anneal temperatures and providing mechanical stability.

This chapter investigates the electrode instabilities and electrode-dielectric interactions with two classes of electrode systems – base metals such as Cu, Ni, Pt and conducting oxides such as lanthanum nickel oxide (LNO). The role of electrode instabilities on dielectric characteristics and yield are studied to obtain optimal process conditions for each system. LNO electrode processes were developed to address the challenges associated with metal electrodes and demonstrate glass-compatible thinfilm capacitors.

3.3 Experimental Methods

Two types of substrates, 200-micron thickness glass and 500-micron thick silicon wafers, were used in this study. Silicon substrates were prepared by depositing silicon oxide on p-type test Si wafers, followed by a thin layer of silicon nitride. Borosilicate glass substrates were used as-received. Two electrode systems were used in this study. The first set of electrodes were formed by sputter-depositing an adhesion layer followed by Cu or Ni as the metal layers. Tantalum was chosen as the adhesion and diffusion barrier between the electrode and silicon.

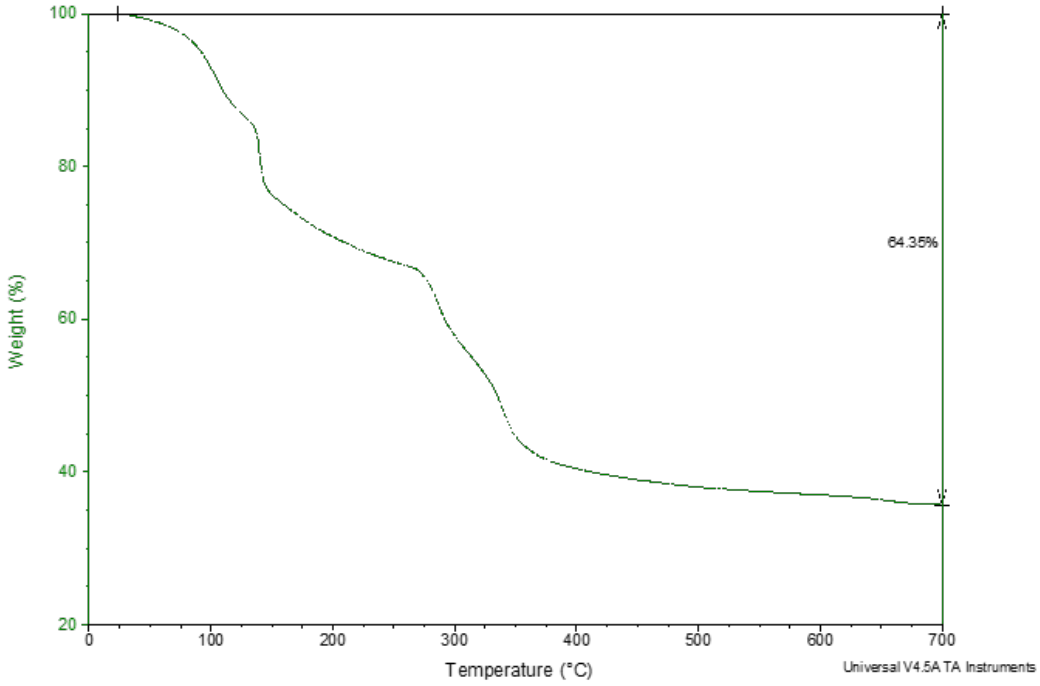


Fig. 3.4: Thermogravimetric analysis to determine the pyrolysis conditions for solgel LNO films.

Conducting oxide electrodes made of lanthanum nickel oxide (LNO) were used as the second electrode system. ZrO_2 was selected as the barrier between the oxide electrode and the glass substrate because of its known effectiveness as a diffusion barrier that

suppresses any chemical interactions between the substrate and electrodes. The LNO film was prepared by dissolving lanthanum nitrate and nickel acetate in methoxy ethanol to form a 0.25M solution. In order to ensure complete dissolution of the precursors with good homogeneity, the solgel solutions were refluxed at 125 C for 6 hrs after each precursor was added. The sol-gel derived LNO were deposited on the substrates using spin-coating for 30s at 4000 RPM (rotations per minute). The coated sample was put on a hot-plate at 400 C for 5 minutes to evaporate the solvents and pyrolyze the volatile components. This process helps to remove all the organics from the film. The pyrolysis conditions were determined from the thermo-gravimetric analysis (TGA) of dried gels. TGA was performed from 25 to 400 C. Fig. 3.4 shows the TGA of LNO indicating significant mass change at 350 C. This shows that bulk of the organics were removed at that temperature.

This spin-coating and thermal treatment processes were repeated 3 times to achieve the target thickness, after which the sample was annealed in air at 650 0C to crystallize the films and improve their conductivity. The resistivity of the film was measured to be 0.1 ohm cm. Multiple coatings were applied in order to increase the thickness and resultant conductivity. After achieving the desired thickness, the sample was post-annealed in an oxygen rich atmosphere to crystallize the LNO. The process flow is shown in Fig. 3.5.

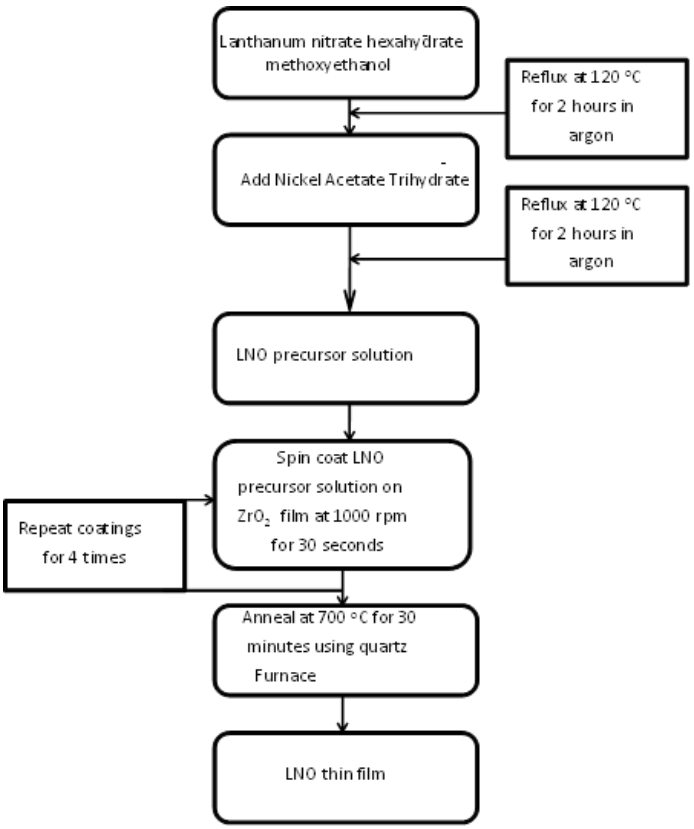


Fig. 3.5: Process flow for synthesis of solgel lanthanum nickel oxide (LNO) films.

The BST thin-films were RF-sputtered on glass substrates using a PVD75 RF sputterer (Kurt J Lesker Inc.). The system was initially pumped down to a pressure of 2 x 10-7 torr. Sputtering was performed in an atmosphere with both oxygen and argon. The oxygen flow was controlled to be 6 s.c.c.m. and the Ar flow was maintained at 4 s.c.c.m. so as to obtain a O2:Ar ratio of 3:2. A pressure of 10 mtorr was maintained in the chamber during the sputtering process at a RF plasma power of 100 W. A three-inch Ba60Sr40TiO3 was used the target. The plasma was sustained for 30 – 60 minutes to obtain films having thickness of 150 or 300 nm, with a sputtering rate of 5 nm/min. The sputtered BST was then post-annealed at 650 C in an oxygen-rich atmosphere for 30

minutes to obtain the perovskite crystal structure. After the annealing process, gold was evaporated using a shadow mask to form the top electrodes.

The capacitance density and loss tangent were measured using a LCR meter (Agilent 4285 Precision LCR meter). Leakage current was characterized using a Keithley 236 DC Analyzer. The insulation resistance was calculated from the measured I-V data. Scanning electron microscopy (SEM) was used to study the surface morphology and perform cross-sectional interfacial characterization. X-ray diffraction (XRD) was used to characterize the crystal structure of the dielectric films. X-ray photoelectron spectroscopy was performed to understand the interactions between the dielectric or electrode structures, as well as study the effectiveness of ZrO2 as the barrier material. Capacitance measurements were performed from room-temperature to 150 oC to obtain the TCC of BST thinfilms (~150 nm).

3.4 Results and Discussion

3.4.1 Structural Characterization:

The X-ray diffraction patterns of barium strontium titanate films crystallized at 700 C are shown in Fig. 5.6, depicting the perovskite structure of polycrystalline barium strontium titanate films. Gold (Au) peaks from the top electrode are also visible in the XRD pattern because the same samples were used for electrical and structural characterization. XRD analysis of the thinfilms showed that all the barium strontium titanate peaks are more intense at higher sintering temperatures implying higher degree of crystallinity. A small amount of pyrochlore phase is detected in some cases as evident from the characteristic 29o peak. In the spectra with metal electrodes, extraneous peaks from metal oxides were also detected.

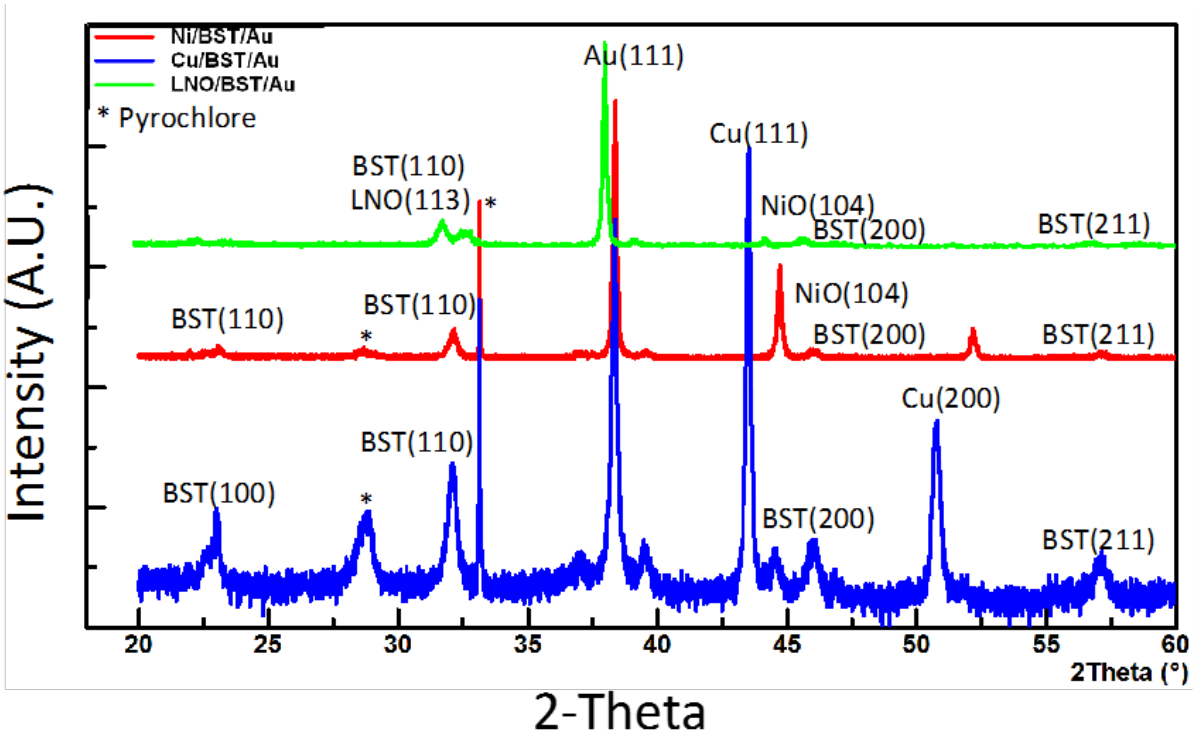


Fig. 3.6: XRD patterns of BST dielectrics from Cu and Ni electrodes.

The films sputtered on copper showed cracks as seen in the SEM images from Fig. 5.7a and 2b. The cracks in the BST, as evident from the SEM, result in high leakage currents, poor yield and reliability. These cracks are attributed to the instabilities in the copper electrode due to stress-relief under annealing, recrystallization and grain growth. They also provide a diffusion path for oxygen to reach the copper surface resulting in subsequent oxidation of the copper. Cu+ ions are known to diffuse to the surface where they get oxidized. The diffusion is aggravated through grain boundaries, pin-holes and other defects. This phenomenon results in an outward oxide growth that eventually forms a hillock. The motion of Cu2+ to the surface also results in voids, as evident in Fig. 3.7c. Tantalum diffusion to the surface has also been observed and is evident in many cases. This is attributed to the high affinity of Ta for oxygen.

Several previous studies have demonstrated copper movement along grain boundaries of the Ta/Si interface when Ta is used as a barrier. In the absence of a barrier between Si and Cu, this Cu reacts with the Si at the elevated post-anneal temperatures to form Cu3Si and subsequently to SiO2 when exposed to oxygen rich atmospheres. The Ta is also known to react with the Si at these elevated temperatures to form h-TaSi2. Hillock formation is also feasible in the absence of oxygen just from the grain coarsening or recrystallization. When hillocks form, the average roughness varies from 50-120 nm.

With films sputtered on Ni electrodes, the hillocking effect was partially suppressed because of the stable electrode structure and interfaces, but still sufficient enough to cause cracks in the films and high leakage when the temperature exceeds 650 ^{o}C. The SEM image in Fig. 3.7d shows the presence of cracks due to the nickel-BST interdiffusion and nickel grain growth. This effect is more predominant when the annealing temperature exceeds 750 C.

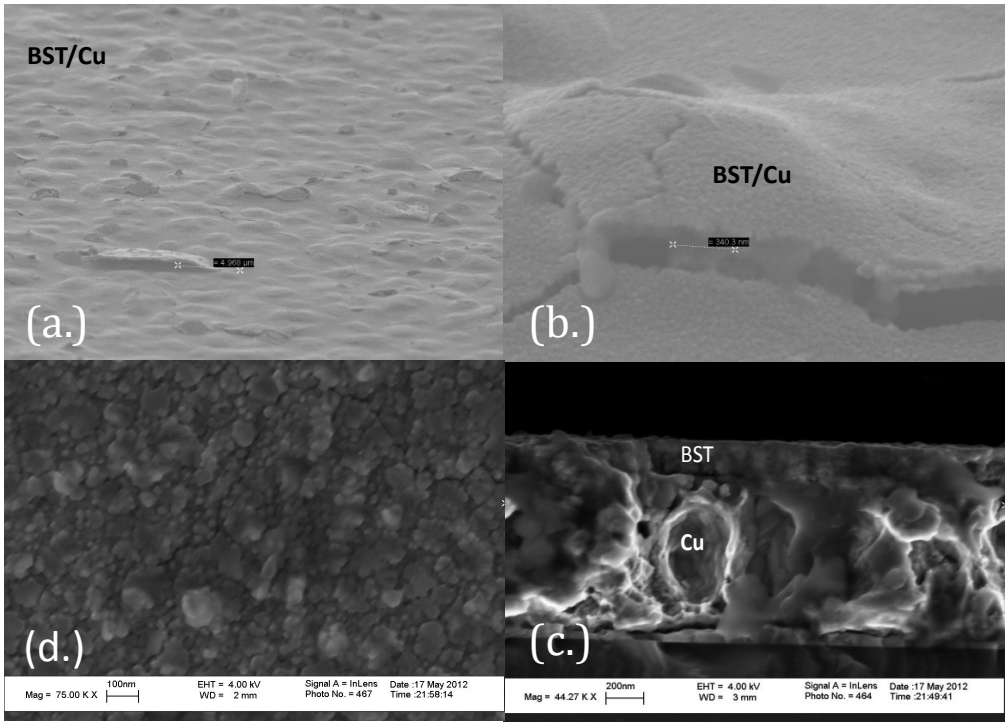
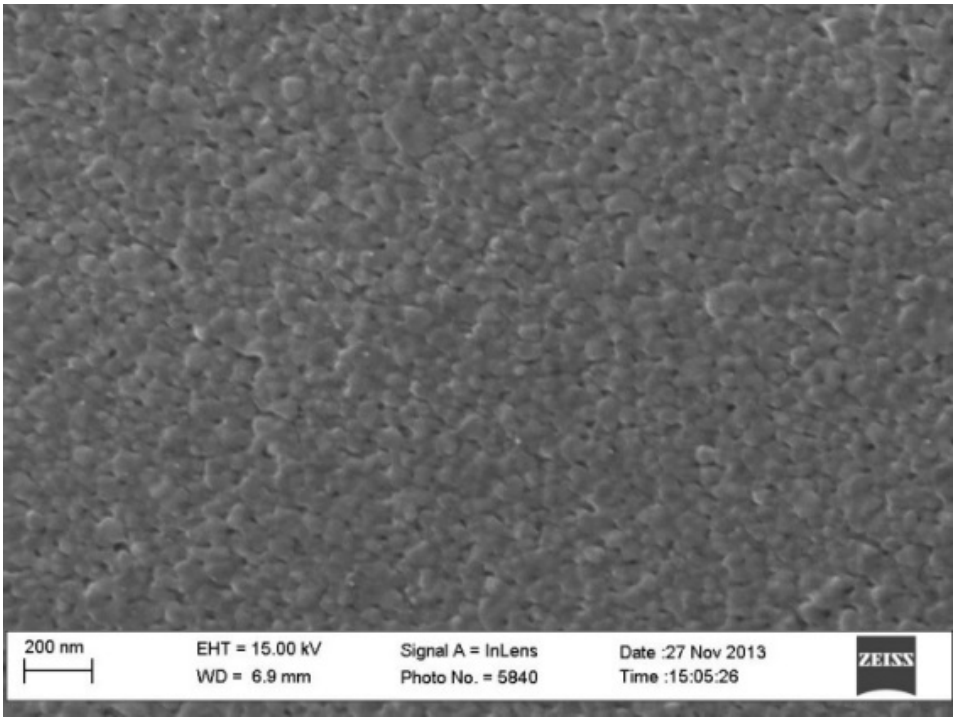
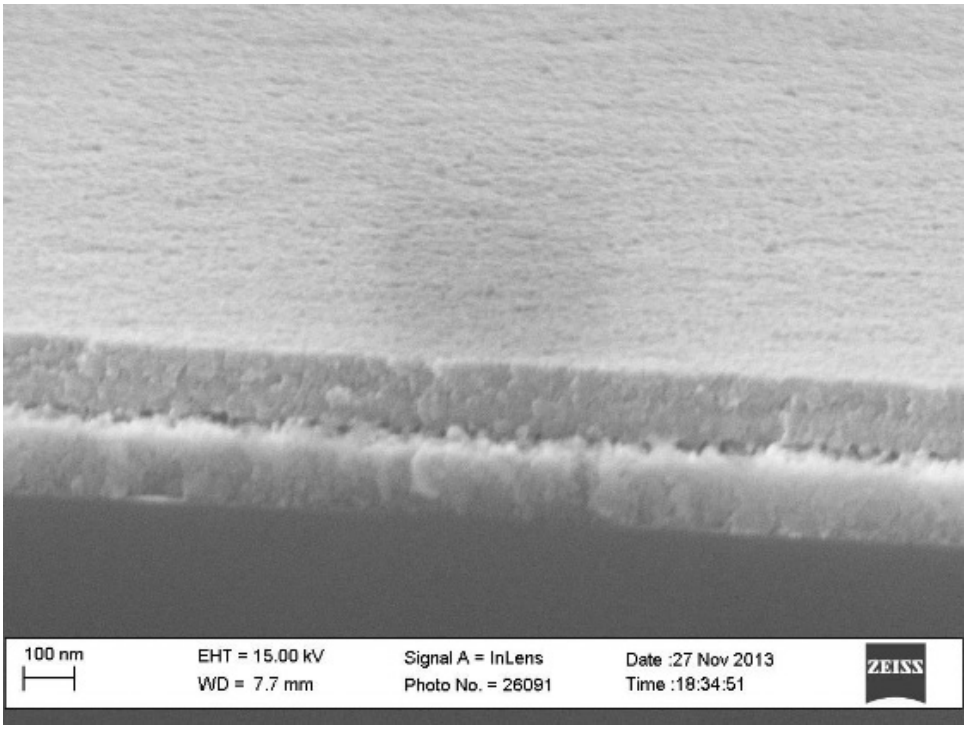


Fig. 3.7: SEM images showing instabilities in BST/Cu and BST/Ni after high-temperature anneal at 700 C. (a.) Large hillocks formed on the BST surface with Cu as the bottom electrode. (b.) Large cracks are evident on the BST surface as a result of hillocks. (c.) A cross-section SEM image showing voids in the Cu and (d.) Cracks in the BST film with Ni as bottom electrode and nickel oxide phases on the surface.

The BST films sputtered on LNO/ZrO2/Si did not show such cracks or heterogeneous grain structure arising from grain growth and recrystallization as is evident in Fig. 3.8. The films showed high yield and low leakage current as compiled in Table 3.1. The LNO forms a stable chemical interface with minimal interfacial reactions and lattice-matched structure as discussed in Section 3.4.2b.



(a.)

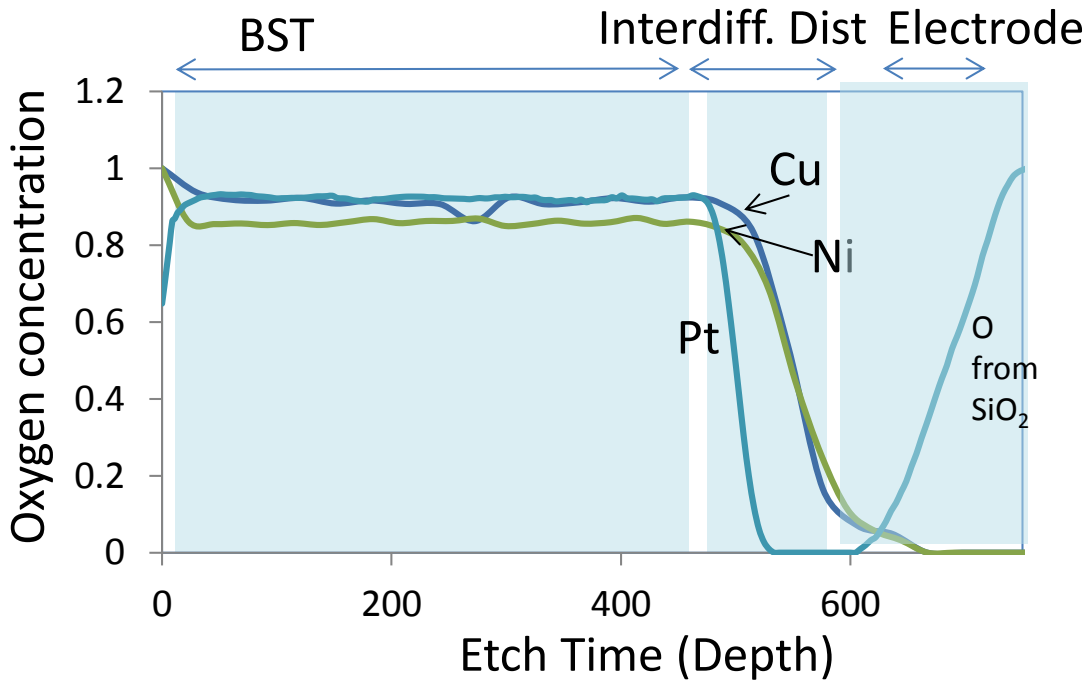


(b.)

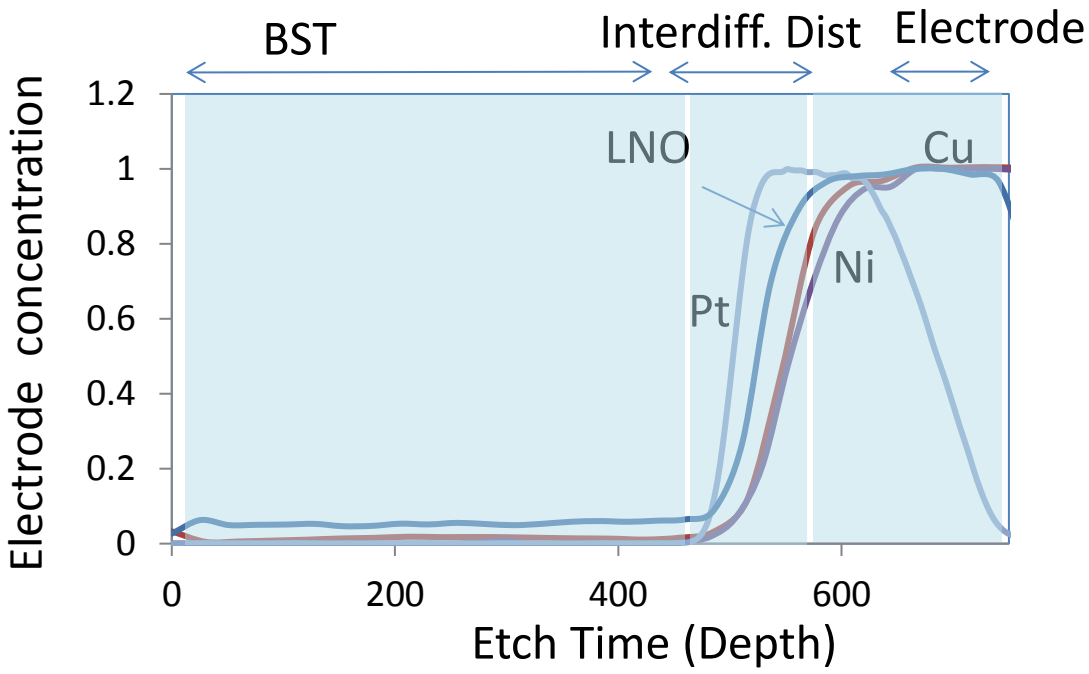
Fig. 3.8: SEM images of sputtered BST on lanthanum nickel oxide electrodes. (a.) Surface morphology of BST on LNO electrode and (b.) cross-section of BST on LNO showing sharp interfaces – indicating no inter-diffusion between the layers.

An XPS depth-profile analysis was conducted to compare the BST interdiffusion distances with Pt, Ni and Cu electrodes. The interdiffusion plots for oxygen and the electrode metal (Pt, Ni (LNO), Ni, and Cu) are shown in Fig. 3.9a and 3.9b respectively. The analysis clearly shows a diffuse interface between the electrode and BST film where the atomic percentages of oxygen stays constant for the dielectric film thickness and gradually decreases with etch-time (representing thickness) when the electrode interface is reached. The distance over which the ions interdiffuse is indicated by the number of etch steps when the concentration gradients are observed. Since the etch rate for the interdiffusion zone varies with each system, only a qualitative comparison can be

obtained from the etch-time or the number of etch steps. The smallest oxygen interdiffusion distances are seen for Pt, followed by Cu and Ni. Similarly, the same trend is observed for the electrode interdiffusion distances. The XPS analysis clearly indicates significant interdiffusion with Cu and Ni compared to Pt. The interdiffusion between LNO and BST is much lower compared to Cu and Ni as seen in Fig. 3.9b. In a previous Cu/barium strontium titanate interdiffusion study with XPS depth-profiling by Kim et al., copper ions were found to diffuse into the dielectric at 200 C but no substantial diffusion was seen at 100 C. The interdiffusion zone acts as a dead-layer with low capacitance and also provides sources for traps that increase the leakage current. Therefore, lower capacitance and higher leakage currents are seen with Cu and Ni as seen in the next section.



(a.)



(b.)

Fig. 3.9: XPS compositional depth profile BST films with various electrodes: (a) Oxygen concentration gradient, (b) Electrode concentration gradient.

3.4.2 Electrical characterization:

3.4.2a BST on Platinum, Copper and Nickel electrodes:

The first set of electrical measurements was performed with BST films on Pt electrodes. After BST deposition, post-annealing was performed at 700 C in the presence of nitrogen. Capacitance densities of ~2 $\mu F/cm^2$, corresponding to a dielectric constant of greater than 750 was achieved with Pt electrodes at an annealing temperature of 700 C. The electrical properties of the BST capacitors from various electrode systems are shown in Table 1. In comparison, a lower capacitance density of 0.7 $\mu F/cm^2$ was achieved for BST/Cu/Ta/SiN/Si planar system. The Cu and BST film thicknesses were ~500 and ~200 nm respectively. The capacitance density, therefore, corresponds to a BST permittivity of ~159. High leakage currents of ~1-2 mA/cm^2 (Fig. 5.11) with this system are consistent with the SEM images from Fig. 3.7. The capacitance densities and leakage currents with BST/Ni/Ta/SiN/Si systems are 1 $\mu F/cm^2$ (corresponding to a permittivity of 227) and 150 $\mu A/cm^2$ respectively, much improved than those from the copper electrodes.

The BST films on Cu and Ni electrodes depicted an opposite trend in capacitance densities with annealing temperatures compared to platinum electrodes. With increasing crystallization temperatures the capacitance values started to drop. Films annealed at temperatures of 450 – 550 C (0.9 – 1 $\mu F/cm^2$) depicted higher permittivities over those annealed at 700 C (0.7 $\mu F/cm^2$). This trend results from the formation of an interface dead-layer of metal oxide between the BST dielectric and base metal electrode. The formation of the dead-layer results in an overall decrease in permittivity. A simple model with two capacitors in series, as seen in Fig. 3.10, can be used to explain the lower permittivity. In the Fig., C_{ideal} is the capacitance obtained from a BST film of thickness 200 nm on Pt electrodes. C_{tot} is the capacitance obtained with Cu or Ni electrodes with a BST film of same thickness. This representation can estimate the capacitance from the

dead-layer ($C_{Cu/Ni}$), which will help isolate the effect of the dead-layer formed because of the base metal oxide between the BST dielectric film and the base metal electrode. It is clear from the equation (3.2) that the effect of the dead-layer capacitance will be more dominant for thinner BST layers and thicker oxide layers.

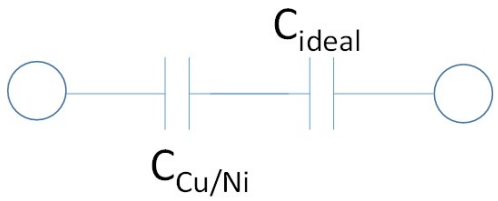


Fig. 3.10: Series capacitor structure formed because of the interface dead-layer between BST and the base metal electrode.

$$C_{Interface} = \frac{C_{ideal} X\ C_{tot}}{C_{ideal} - C_{tot}} \quad (3.2)$$

The estimated interface dead-layer and film capacitances for Cu electrodes are 0.91 μF/cm^2 and 0.7 μF/cm^2 respectively, while those with Ni electrodes are 1.5 μF/cm^2 and 1 μF/cm^2. It is important to note that this phenomenon is observed even though the BST films on Cu and Ni electrodes annealed at temperatures of 700 C have better crystallinity as compared to those at 450 C.

The leakage current data on base metal electrodes also demonstrated opposite behavior to that seen on Pt electrodes. BST films on Pt electrodes have reduced leakage currents and dielectric loss after a high temperature post-anneal. However, in the case of Cu or Ni electrodes, an increase in both leakage current and dielectric loss has been observed. This can be attributed to the significant grain growth that is observed after post-annealing at temperatures of 700 C. This grain growth and subsequent hillock formation is more

evident in copper compared to nickel as discussed in the previous sections. Consistent with the observed microstructures, higher leakage current and losses were observed in BST films on Cu compared to those grown on Ni. The aforementioned effects also affect the overall capacitor yield. As is evident from the data in Table 3.1, BST films on Cu had the lowest yield ~40%, whereas Ni had a yield of almost 60%.

3.4.2b BST on Lanthanum Nickel Oxide Electrodes:

The electrical performance from Cu and Ni-based electrodes was compared with that from LNO electrodes deposited on Si with ZrO2 film as the barrier. LNO diffusion into the silicon is prevented by using zirconia as the barrier. Capacitors formed using LNO as the bottom electrode showed superior properties relative to those prepared with Cu and Ni. With LNO/ZrO2/Si as the bottom electrode, capacitance density was found to be 1.5-2 $\mu F/cm^2$ (corresponding to a permittivity of 455) with 95% yield, as shown in Table 3.1. The LNO/BST electrode-dielectric system formed crack-free films with lower inter-diffusion between the electrode and dielectric compared to those with Cu and Ni as seen in Fig. 3.8. Higher capacitance density and relatively lower leakage current values compared to the Cu and Ni systems are attributed to stable interfaces and crack-free films. A comparison of the leakage current data obtained from Cu, Ni and LNO electrodes is plotted in Fig. 3.11. The surface roughness and inhomogeneous microstructure contributes to the leakage currents. With smooth LNO films from improved sol-gel process, the electrical performance can be further improved. The capacitance density and leakage current were found to be similar to those found with Pt electrodes.

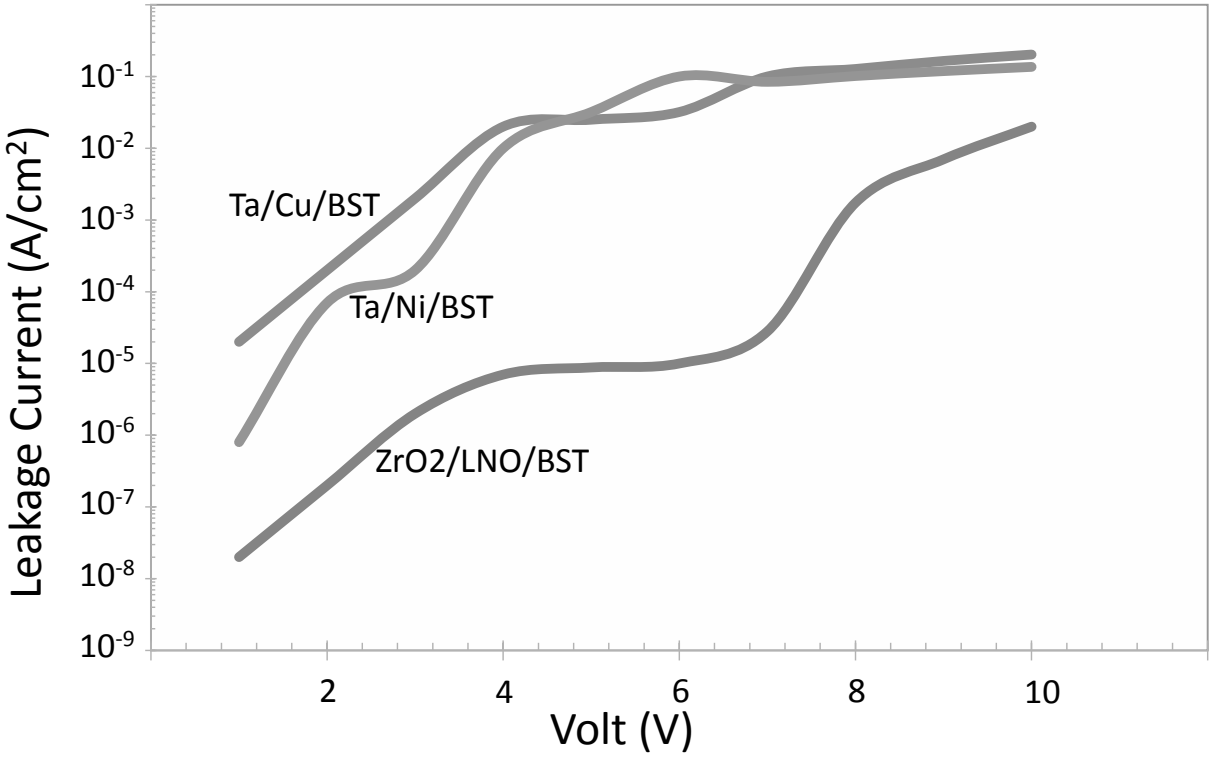


Fig. 3.11: Leakage current plots for Cu, Ni and LNO electrodes.

Table 3.1: Electrical properties and yield as affected by two electrode systems.

	Metal Electrodes		Conducting Oxide Electrode
	Ta/Cu/BST	Ta/Ni/BST	ZrO2/LNO/BST
Annealing conditions	700 C, 30 min in N_2	700 C, 30 min in N_2	700 C 30 min in O_2
Capacitance density	7-8 nF/mm^2	9-11 nF/mm^2	15-20 nF/mm^2
Leakage current of the order	1-2 mA/cm^2	100 – 150 μA/cm^2	3 – 4 μA/cm^2
Yield	40% (14/35 devices yielded)	57% (20/35 devices yielded)	95% (33/35 devices yielded)

3.5 Summary

Capacitance density and leakage current characteristics of silicon and glass-compatible thin-film decoupling capacitors were investigated with two different electrode systems; base metal such as Cu or Ni and conductive oxides such as LNO. With sputtered-copper metal electrodes, the instability at the electrode-dielectric interfaces creates macroscopic and microscopic defects in the dielectrics after annealing. This results in poor electrical performance and yield unless suitable barriers are utilized between the metal-dielectric and metal-substrate interfaces. Nickel electrodes, on the other hand, showed lower leakage currents and higher capacitance densities though the annealing temperature was limited to 700 C. The instabilities in this case are related to hillock formation during thermal stress relief, oxygen diffusion and recrystallization. These instabilities are more predominant with copper electrodes compared to nickel. Conducting oxide electrodes, on the other hand, showed stable interfaces resulting in higher capacitance densities and lower leakage currents. This is attributed to the improved thermal and interfacial stability of these electrodes. This work, thus, provides the first demonstration of thinfilm capacitors on ultra-thin glass substrates with high capacitance density and low leakage.

CHAPTER 4

HIGH DENSITY SI-NANOWIRE CAPACITORS

4.1 Introduction:

Thinfilm capacitors, discussed in Chapter 3, are limited to capacitance densities of ~30 nF/mm^2 and are, therefore, effective in addressing high-frequency switching noise in power supplies where the required capacitances are low. Much higher capacitance densities (30-100X) are needed for filtering noise from lower-frequency harmonics that are typically seen in power supplies such as switching regulators. High surface area electrodes are one way to achieve such high capacitance densities in conjunction with very thin dielectrics. This chapter describes Si-nanowires for such high-density capacitors. In spite of their low-permittivity, silicon-integrated nanowire capacitors are advantageous because they can be processed to nanoscale with extremely high aspect ratio.

The chapter is organized as follows: Section 2 presents analytical models to determine the geometry, frequency stability and voltage levels to achieve maximum capacitance in silicon capacitors. Section 3 describes the fabrication process. Section 4 presents the characterization results and Section 5 summarizes the key findings.

4.2 Background On Silicon-Based Nanocapacitors:

Trench-based silicon capacitors were developed at IBM in 1980s for volatile memory applications (DRAMs). The trench shape and structure defines the surface area that is available to form the capacitor. The trenches are created by reactive ion etching of silicon while the dielectrics are formed by thermal growth of oxides or oxynitrides. An example

of a cross-section of the trench capacitor is shown in Fig. 4.1. Pores, cylinders and tripods have all been explored to achieve high capacitance densities. IPDiA, for example, has shown that hexagonal tripod structures with extremely high aspect ratio of above 100 have the potential of achieving 1 $\mu F/mm^2$. Combining higher-permittivity dielectrics such as Al_2O_3, HfO_2, ZrO_2, BT, BST, etc. with the trench structures can further increase the capacitance. The main challenge with the trench capacitors is to be able to deposit these high aspect ratio structures conformally without any pinholes or defects. ALD has commonly been employed to deposit alumina and hafnia thinfilms that are of high quality and defect free. Multilayer approach to form capacitors one above the other and connected in parallel is also being explored as an alternative to achieve high capacitance densities with trench structures. This has been demonstrated with multiple layers of TiN/Al_2O_3. However, it should be noted that such a process requires multiple masks and several ALD steps. With advances in trench formation and dielectric deposition processes, capacitance densities of above 1 $\mu F/mm^2$ have been achieved [39, 48].

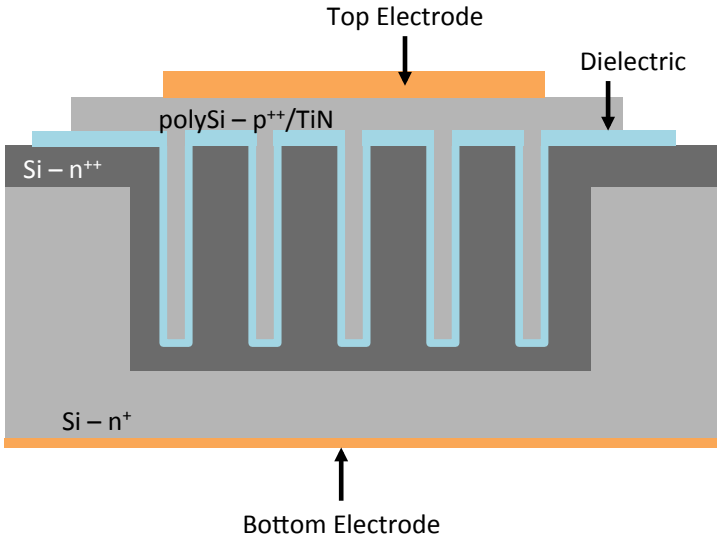


Fig. 4.1: Schematic representation of trench capacitor structure in Si.

Silicon Nanowires: Nano-structures such as Si-nanowires are being studied to investigate their potential. Nanowires were explored for the first time in the 1960s using chemical vapor deposition (CVD) with molten metal catalyst droplets. This technique is also frequently referred to as vapor-liquid-solid (VLS) approach [73-78]. This process uses CVD in conjunction with metal nano-particles to form a low-temperature eutectic liquid with Si. The silicon vapor adsorbs onto the molten metal, forms a supersaturated solution facilitating easier nucleation and crystal growth. The most preferred metals are Gold (Au) and Silver (Ag). This is because they form eutectics at relatively low temperatures compared to other metals. Gold forms a eutectic with Si at 373^{O} C as can be seen in the phase diagram in Fig. 4.2. Physical deposition methods such as laser ablation, e-beam evaporation or molecular beam epitaxy are used to facilitate growth. A general schematic of nanowire growth is shown in Fig. 4.3 [79, 80].

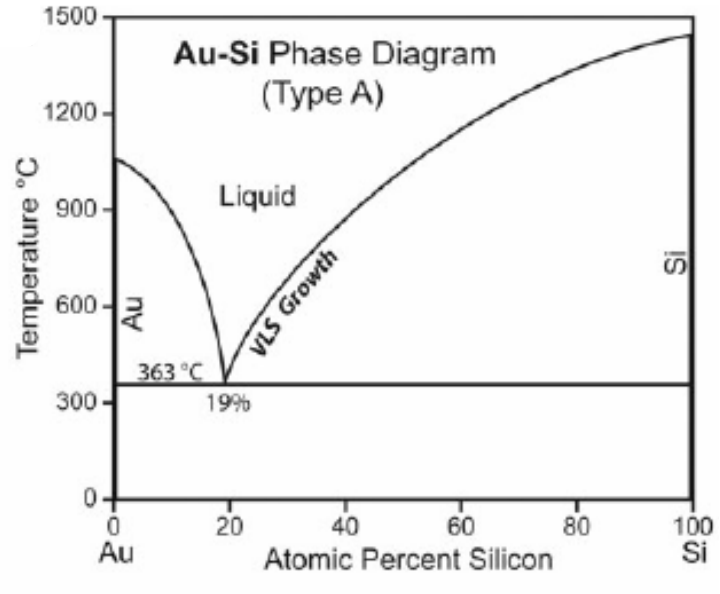


Fig. 4.2: Au-Si Phase diagram [79]

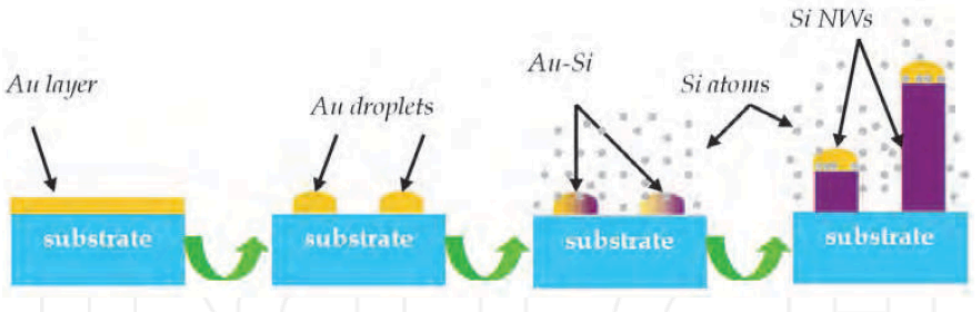


Fig. 4.3: Schematic representation of Si nanowire growth using Au as a catalyst [79].

An alternative method to form Si-nanowires is based on a wet-etch process. This process is relatively less complex and lower cost, as it does not require the precursors, vacuum chambers or tight control on temperature and pressure to fabricate these structures. This process has been perfected both on bulk Si and thin Si. Wet etching of the nanowires preserves the bulk Si properties in the structures. Hence, ultra-low resistance wires can be achieved by simply having a large doping concentration. The most common form of etching is using a metal as a catalyst. Silver and gold are the primary choices as the energy levels of Ag+/Ag0 and Au+/Au0 are lower than the Si valence band. Reactions when using Ag as the catalyst are highlighted below.

$$Ag^{+}(aq) + e_{-VB,\,Si} \rightarrow Ag^{0}\,(solid) \qquad (4.1)$$

$$Si\,(solid) + 2H_2O - 4e_{-VB,\,Si} \rightarrow SiO_2\,(solid) + 4H^{+} \qquad (4.2)$$

$$SiO_2\,(solid) + 6HF \rightarrow H_2SiF_6 + H_2O \qquad (4.3)$$

The Si below the Ag0 gets oxidized to form SiO_2. The oxide readily dissolves in the HF acid, creating a small void into which the catalyst drops. The Ag^0 attracts more of Ag^+. These accumulated ions are then reduced to Ag leading to their accumulation in the pits.

These particles do not move and become centers where the redox reaction continuously occurs to form nanowires. At room temperature and pressure, the length of the wires is limited to 50 μm. This limitation is overcome by moving to more complex etching chemistries [79,80].

4.3 Analytical Modeling of Si Nanowire Capacitors:

The objective of analytical modeling is to estimate the silicon nanowire geometry, capacitance density and frequency- stability from first principles. Silicon nanowire capacitors are essentially metal-oxide-semiconductor type capacitors. The capacitance of a MOS structure depends on the voltage bias applied to the metal (gate). The capacitor can operate in three different states based on the voltage applied. The states can be classified as (i) Accumulation: Surface accumulation of carriers that are same as the majority carriers in the bulk, (ii) Depletion: No carriers present on the surface with only a space charge or depletion region is present and (iii) Inversion: Opposite charge carriers to those present on the body accumulate on the surface. Two voltages can be used to effectively separate these three different regions. These are (a) Flatband Voltage: It helps separate the accumulation region from the depletion region and (b) Threshold voltage: Helps separate the depletion region from the inversion region. This paper focuses only on the accumulation region for a MOS capacitor. Based on the calculated capacitance and resistance, the RC time constant for such capacitors can be estimated.

4.3.1 Nanowire Length Approximation:

When Au is used as a catalyst, the nanowire length can be estimated using Equation 4.4, where L is the length of the nanowire, r is the radius at the base, a3 is the atomic volume of Au and theta is the average Au coverage on the sidewalls. Theta has been estimated to be 1 – 1.5 monolayers [81]. Table 4.2 summarizes the approximate length of nanowires that can be grown based of the Au catalyst size.

$$L = \frac{r^2}{2a\theta} \text{ [81]} \qquad (4.4)$$

4.3.2 Nanowire Resistance:

Knowing the conductivity of the silicon, the resistance of the nanowires can be estimated. The following equations are used to calculate the resistance based on the doping concentration.

$$R = \frac{\Delta l}{\sigma S} \qquad (4.5)$$

Where R is the resistance in ohms, Δl is the length of the nanowire in meters, σ is the conductivity in Siemens/m and S is the cross-sectional area of the nanowire. The conductivity of an intrinsic semiconductor is defined as:

$$\sigma = n_i(\mu_e + \mu_h)q \qquad (4.6)$$

where n_i is the intrinsic carrier concentration, q is the charge of the electron (1.6×10^{-19} C), and μ_e and μ_h are the mobilities of the electrons and holes respectively. For an extrinsically doped semiconductor, either the electron or hole concentrations dominate and hence the other can be ignored while calculating the conductivity. It is well known that there is no net charge for an intrinsic semiconductor. This remains same even for

extrinsically doped semiconductors. This means that even after doping, the total number of positive charges equals the total number of negative charges. This is derived from the Mass-Action law, which states that

$$np = {n_i}^2 \qquad (4.7)$$

For extrinsically doped n-type semiconductor:

$$\sigma = n\mu_e q \qquad (4.8)$$

For extrinsically doped p-type semiconductor:

$$\sigma = n\mu_h q \qquad (4.9)$$

where n in the above equations can be replaced with N_D or N_A based on the doping type. Using the equations specified above, the required donor concentrations required to achieve 5 ohm-cm and 10 ohm-cm are seen in Table 4.1.

Table 4.1: Doping concentrations for both p-type and n-type semiconductors to achieve 5 and 10 ohm-cm resistivity.

Resistivity	P-type doping concentration (cm^{-3})	N-type doping concentration (cm^{-3})
5 ohm-cm	$2.5x10^{15}$	$1\ x10^{15}$
10 ohm- cm	$1.4x10^{15}$	$0.45\ x10^{15}$

This chapter assumes a p-type Si substrate for all further analysis. The volumetric capacitance density was calculated based on the capacitance from Table 4.2. A conformal

SiO2 dielectric with a dielectric constant of 4 and a dielectric thickness of 10 nm was considered for the calculation. The capacitance of a cylinder is calculated as:

$$C = \frac{2\pi\varepsilon_o\varepsilon_r * l}{\ln \frac{b}{a}} \qquad (4.10)$$

Where "a" is the inner diameter and b is the outer diameter.

Table 4.2: Analytical modeling data showing capacitance and cut-off frequency as a function of Au catalyst size.

Si-type	Au catalyst size (nm)	Length of wire (μm)	Resistance (Mohms)	Capacitance (fF)	RC time constant (nS)	Cut-off Frequency (MHz)
5 ohm-cm	30	1.731	30	2.2	66	2.4
	50	4.8	31	9.4	300	0.5
	100	19.23	31	70	210	0.075
10 ohm-cm	30	1.731	60	2.2	132	1.2
	50	4.8	62	9.4	600	0.26
	100	19.23	62	70	4200	0.0375

The total number of nanowires per unit area was estimated based on the nanowire diameter and minimum distance between wires. The density was estimated to be 100 – 150 μF/mm^3. This capacitance value is about 10X higher than current capacitor technologies, and 2X higher than what is projected as the maximum achievable density with existing capacitor technologies.

Based on the above equations, the capacitance and resistance are calculated and the RC time constant can be estimated as

$$\tau = RC \qquad (4.11)$$

And the cut-off frequency is estimated as

$$\tau = \frac{1}{2\pi f_c} \qquad (4.12)$$

$$f_c = \frac{1}{2\pi\tau} \qquad (4.13)$$

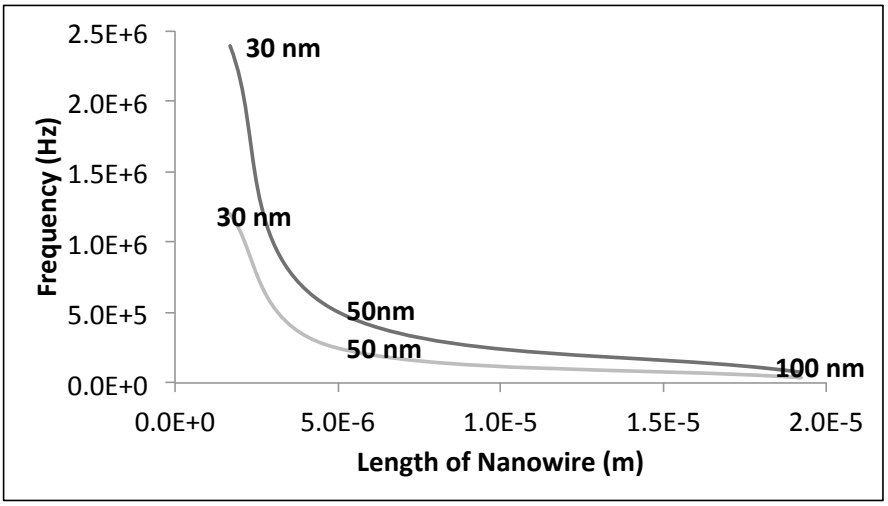


Fig. 4.4: Change in cut-off frequency with increasing nanowire length.

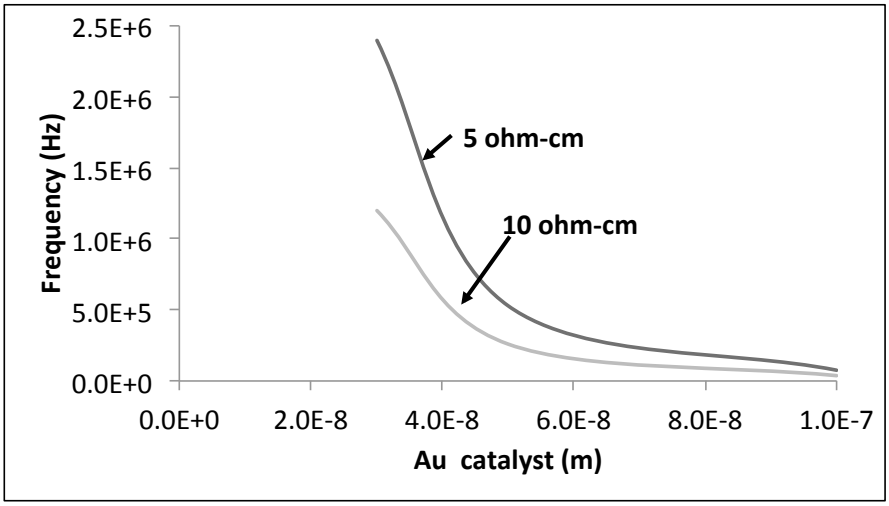


Fig. 4.5: Change in cut-off frequency with respect to Au catalyst size.

4.3.3 Cut-off frequency:

Cut-off frequency, the frequency above which the capacitor performance degrades, is an important factor in power supply design. Using Equations (4.11-4.13), Fig. 4.4 and Fig. 4.5 show the cut-off frequency with changing wire length and catalyst size respectively. The cut-off frequency is inversely proportional to increasing R and C. Hence, with increasing wire length, both resistance and capacitance increase but cut-off frequency decreases.

4.3.4 Flatband voltage:

The flatband voltage is the voltage at which no charge is present on the capacitor electrodes leading to no electric field across electrodes. This phenomenon takes place when the applied voltage is greater than the flatband voltage (positive or negative depends on substrate type). The flatband voltage depends on the doping concentration of Si. It is also highly- dependent on any residual charge that may be present at the interfaces and across the electrodes. Hence, when a voltage greater than the flatband (large negative voltage for a p-type substrate) voltage is applied, it causes the holes to be attracted to the interface causing accumulation. The opposite is true for an n-type substrate [82]. Analytically modeled values for flat-band and threshold voltages are seen in Table 4.3.

$$V_{FB} = \phi_m - \phi_s \tag{4.14}$$

$$\phi_s = \chi - \frac{E_g}{2q} - V_t Ln\left(\frac{N_a}{n_i}\right) \tag{4.15}$$

$$\phi_s = \chi - \frac{E_g}{2q} + V_t Ln\left(\frac{N_d}{n_i}\right) \quad (4.16)$$

$$V_t = \frac{KT}{q} \quad (4.17)$$

A p-type substrate is considered in this analysis; hence the threshold voltage is defined as

$$V_T = V_{FB} + 2\phi_F + \frac{\sqrt{4\varepsilon_s N_a \phi_F}}{C_{ox}} \quad (4.18)$$

$$C_{ox} = \frac{\varepsilon_o \varepsilon_r A}{d} \quad (4.19)$$

where Φm is the work-function of the metal gate, Φs is the work-function of Si, χ is the electron affinity, ΦF is the bulk potential of Si, εs is the relative permittivity of Si, Cox is the oxide capacitance (under accumulation), K is the Boltzmann's constant, T is the temperature in K and q is the charge of an electron in C. It is important to calculate the threshold voltage and the flatband voltage, as this will allow capacitor operation in accumulation, resulting in maximum capacitance [83, 84]. The voltage dependence of MOS capacitance is shown in Fig.4. 6.

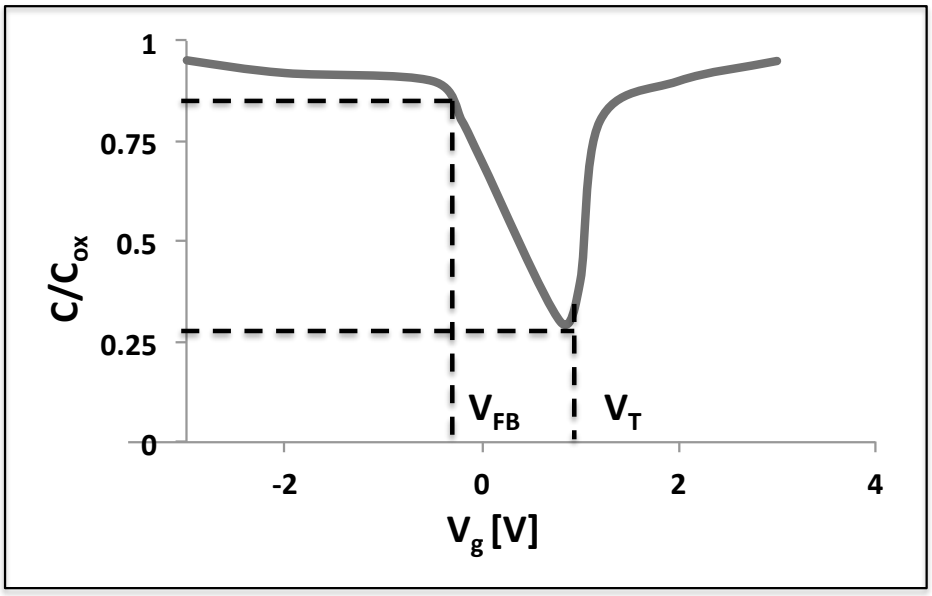


Fig. 4.6: Voltage dependence of MOS capacitance.

Table 4.3: Analytical flatband and threshold voltages

	Copper	N^+ Poly	P^+ Poly
V_{FB} (V)	-0.36	-0.87	0.23
V_T	0.37	-0.14	0.96

4.4 Fabrication:

Capacitors were fabricated with Si-nanowires as the bottom electrode, thin-oxide as the dielectric and PEDOT:PSS (poly(4,5 ethylene dioxy thiophene) – poly(styrene sulphonate)) as the top electrode. The nanowires were fabricated using two different techniques: 1. CVD growth and 2. Etching. The oxide was formed using a thermal oxidation technique and finally the top electrode was formed by dispensing PEDOT:PSS nanosuspension. Next, each of the steps in the fabrication process is explained in detail. A schematic of the entire fabrication process is seen in Fig. 4.7.

4.4.1 Nanowire Fabrication:

The bottom electrode of the capacitor was formed by the nanowires. Nanowire fabrication was carried out using two different methods.

4.4.1.a CVD Growth:

The experiments to grow Si nanowires were carried out using a CVD furnace. The nanowires were grown on a Si(111) substrate. The substrate was cleaned to remove any natural oxide using 10% hydrofluoric acid. Gold catalyst was then deposited using a colloidal gold suspension. This allows for the Au to be distributed on the substrate. Gold particles with various diameters were used as the gold catalyst. It was seen that the 50 nm particles consistently produced nanowires. The substrate with gold catalyst was placed in the CVD chamber. The temperature was maintained between 410 – 430 oC. A mixture of silane gas (15%) and hydrogen gas (85%) (Carrier) was used. The process was run for 10 minutes. The nanowires grown from these experiments are completely random in orientation. More control over the process parameters can yield more directional wires. For capacitors, the random orientation of the wires can be an advantage as they provides= considerably more surface area than vertical wires and increases the overall capacitance density. Hence, there was no further effort to improve the orientation of the nanowires.

4.4.1b Etching:

An alternative approach based on etching process was also utilized to form the Si nanowires. The etching process uses Au as the catalyst, which is then patterned into nanoscale islands using e-beam nanolithography. It was seen that the gold was more stable compared to colloidal gold catalyst used for the CVD process. It did not move and diffuse into other gold droplets. The etching solutions consisted of a mixture of hydrofluoric acid and hydrogen peroxide. The Si was etched only in locations were Au catalyst was present, leaving the Si around it unaffected. This allowed for extremely

vertical Si nanowires. This process requires more control than the CVD process as any change in the etching mixture could result in unwanted etching and pit formation on the Si surface. This is highly undesirable when trying to achieve high aspect ratio structures.

4.4.2 Oxidation:

The next step in the capacitor fabrication process after nanowire fabrication is the formation of the dielectric. Silicon oxide has the highest electric breakdown strength because of its large bandgap, making it withstand sufficient voltages even when thinned down to 10s of nm. It is also important to note that the deposition of high-k dielectrics such as barium strontium titanate in high-aspect ratio structures such as these nanowires would be extremely challenging. Hence, silicon oxide was the dielectric of choice for these capacitors using a novel technique for low-temperature (<500 C) oxidation.

4.4.3 Top Electrode using PEDOT:PSS

Conducting polymer (PEDOT:PSS – poly(4,5 ethylene dioxy thiophene) – poly(styrene sulphonate)) was used as the cathode for the silicon-nanowire systems. PEDOT:PSS is the most widely used conducting polymer in the capacitor industry. PEDOT:PSS has a high conductivity (~600 S/cm), which results in extremely low ESR compared to other cathodes such as MnO2 and is self-healing in nature. Self-healing in PEDOT:PSS leads to burning of the cathode next to a defect site in dielectric, thus, preventing a short between the cathode and the anode. This also helps in minimizing the leakage current.

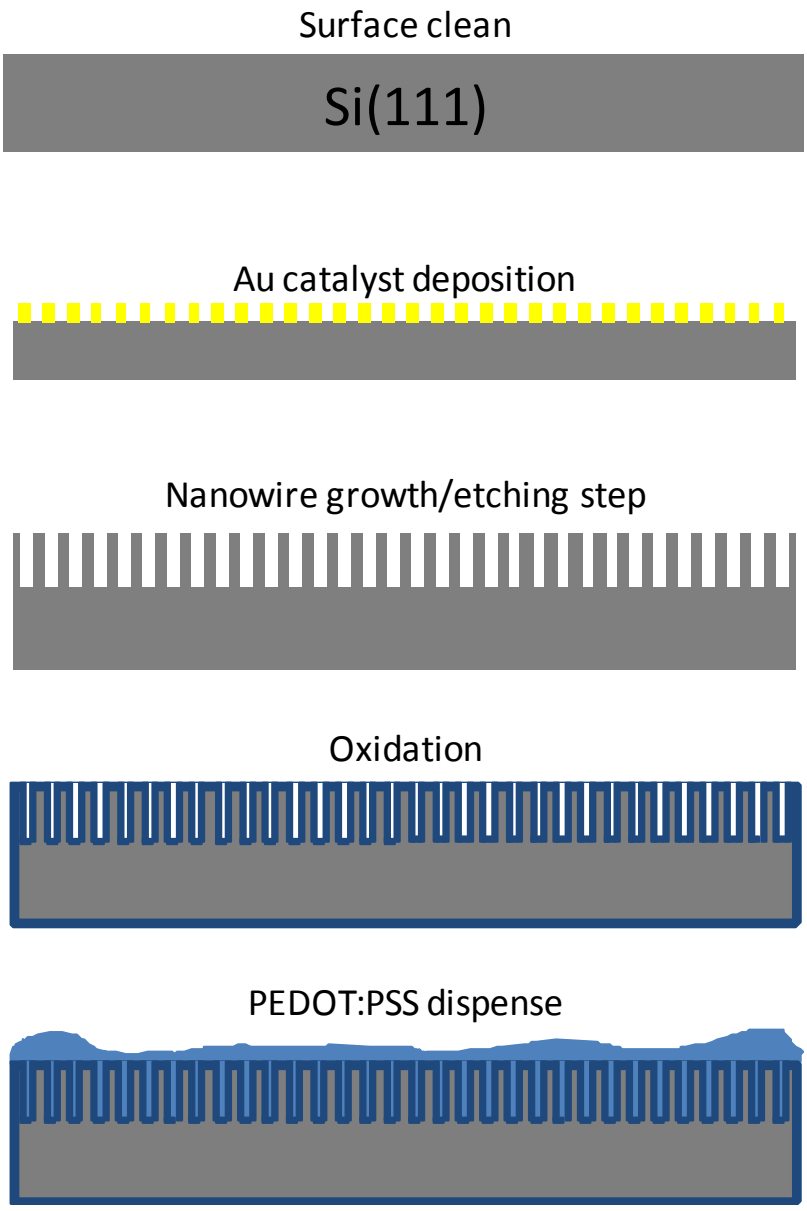


Fig. 4.7: Fabrication process for Nanowire capacitor formation

4.5 Characterization

The morphology of the nanowires was studied using scanning electron microscopy (SEM). The oxide was studied using SEM and X-ray photon spectroscopy (XPS). The capacitor was tested using a liquid electrolyte as the cathode. Each step is briefly discussed below.

4.5.1 Morphology of Si-Nanowires

The Si-nanowire samples were characterized using scanning electron microscopy (SEM) to study the morphology. It was seen that nanowires that were grown using the VLS (Vapor-Liquid-Solid) technique in the CVD chamber were randomly oriented. This is desirable as the resultant porous structure allows for extremely high surface area that can lead to very high capacitance density. SEM image of the randomly-oriented nanowires is shown in Fig. 4.8. The length of the nanowires was measured to be around 3 – 3.5 micron, with Au catalyst sizes of 50 nm. The analytical modeling shows that the length should be around 5 micron. The limited growth is attributed to the small processing times used (< 10 minutes). Nanowires formed using the etching processes were also characterized, as shown in Fig. 4.9. It was seen that the wires in this case were completely vertical. The length of all the wires was almost the same, indicating minimal standard deviation. In case of the etching process, the length of the wires was highly dependent on the etching times.

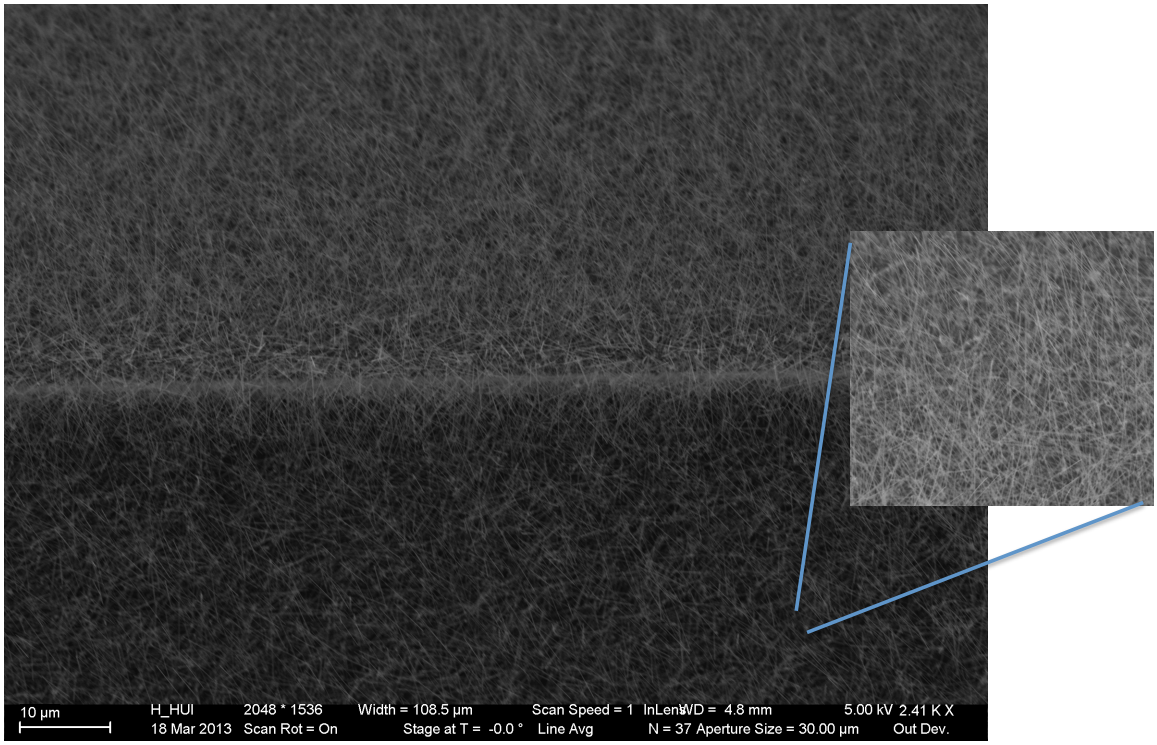


Fig. 4.8. Morphology of CVD Si-nanowires using FE-SEM. Image shows randomly orientated nanowires.

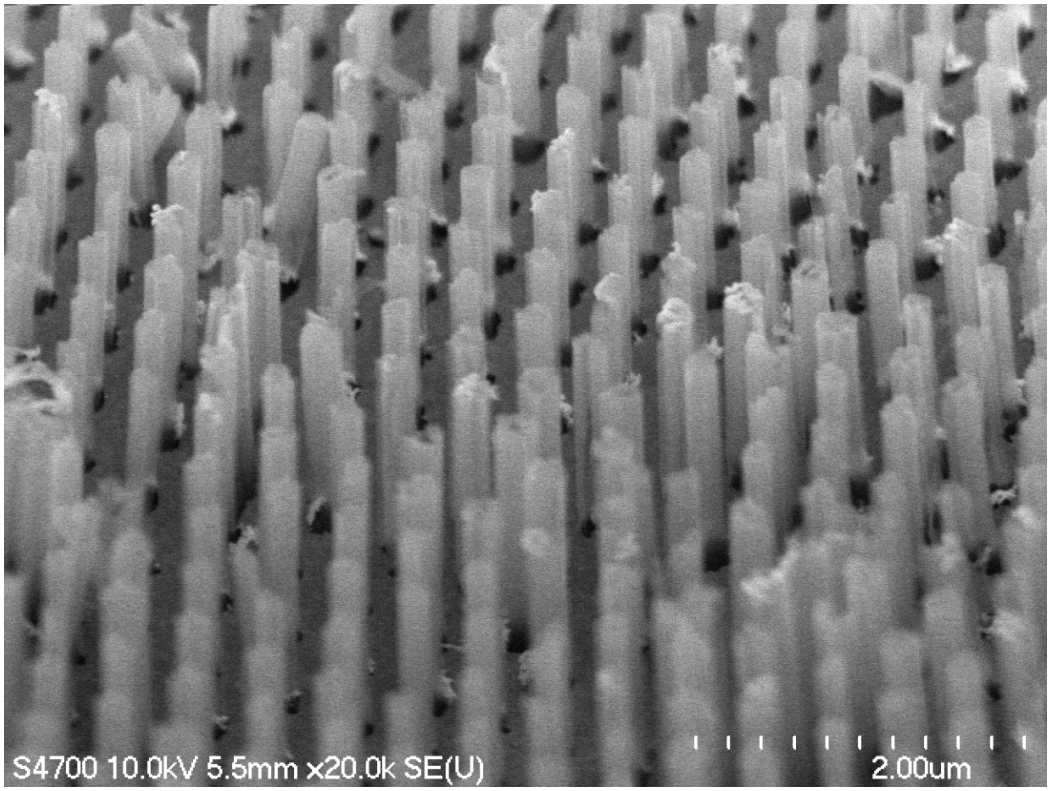


Fig. 4.9. Morphology of Si-nanowires using FE-SEM.

4.5.2 Capacitor Characterization

The fabricated devices were characterized for capacitance and leakage currents. For measuring the ideal capacitance density of the device utilizing all the electrode area, liquid electrolyte testing with a set-up shown in Fig. 4.10 was used. The silicon nanowire capacitor was used as the anode whereas sulfuric acid with a concentration of 0.5 M was used as the electrolyte, in addition to working as a cathode. The presence of an electrolyte leads to additional capacitance due to the formation of the electrochemical double layer at the oxide-electrolyte interface. A schematic of the interfaces involved in the capacitor system is presented in Fig. 4.10 to illustrate the capacitance contribution from the silicon oxide and the electrochemical double layer. As seen from the Fig., the capacitance contribution from the double layer and the oxide are in series. With such series

capacitors, the smaller capacitor dominates the capacitance. The net capacitance for this capacitor series is therefore determined by the contribution from the nanowire because the double-layer capacitance is much higher. The capacitance is calculated as:

$$C = \frac{A\varepsilon\varepsilon_r}{t} \qquad (4.20)$$

where A = Surface area of the electrode, ε = Permittivity in vacuum, εr = Relative permittivity of the dielectric, and t = thickness of the dielectric.

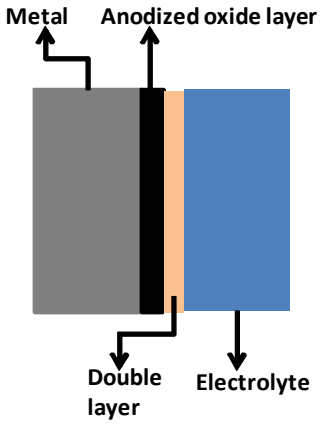


Fig. 4.10 Interface involving two dielectrics in the wet-system (metal oxide and electrochemical double layer) [85].

Assuming the surface area (A) of the double-layer and oxide capacitors to be the same, εr1 and t1 = permittivity and thickness of the oxide layer, εr2 and t2= permittivity and thickness of the double layer, C1 = capacitance from the oxide layer, C2 = capacitance from the double layer;

$$\varepsilon_{r1} << \varepsilon_{r2}; \quad t_2 << t_1 \Rightarrow C_1 << C_2$$

Here, since C1 and C2 are in series,

$$C_{eff} = \frac{(C_1 \times C_2)}{(C_1 + C_2)} \cong C_1 \qquad (4.21)$$

The capacitance measurement obtained using this set-up can be approximated as the capacitance from the silicon nanowire electrode.

The measurement results showed a maximum capacitance density of 20 $\mu F/cm^2$ with liquid-electrolyte testing. A leakage current of 1 $\mu A/\mu F$ was recorded. When compared to planar silicon oxide capacitors with 50 nm oxide films, this approximates to a 40 X enhancement in surface area in spite of being only 2 microns thin. The nanowire electrodes result in a high volumetric density compared to other thin capacitor approaches. As seen in Fig. s 4.4 and 4.5, it is estimated that the capacitors will be limited in frequency performance to low kHz. This is attributed to the extremely high resistance of the nanowires with test silicon wafers (1-10 ohm cm resistivity). With low-resistivity doped silicon, the conductivity can be further enhanced to improve the operation frequency of these capacitors.

Compared to alternative substrate-compatible high surface area electrode techniques such as trench capacitors or nanoparticle electrodes, the etched nanoelectrode process is much simpler and allows easy scale-up at low cost. The results therefore represent a significant breakthrough and advance in nanocapacitor technologies.

4.6 Summary

A novel process to achieve ultrahigh-density capacitors was demonstrated using Si nanowire electrodes. An analytical model was developed to predict the length of the nanowire, the capacitance density and frequency-stability that can be achieved with the nanowire structures. The flatband voltage and the threshold voltage were also calculated. This helps to determine the required voltage for the MOS device to operate in accumulation mode for maximum capacitance density.

Nanowires were formed using two distinct processes: 1). VLS growth technique using CVD and 2) Wet-etching process. SEM was used to characterize the wires. The VLS growth technique produced randomly-oriented wires that are desirable as they enable very high capacitance densities. The etching process, on the other hand, provided vertical nanowires. Thin oxides were grown using thermal oxidation process. Finally, top electrodes were formed using PEDOT:PSS (conducting polymer). A capacitance density of 20 $\mu F/cm^2$ was measured for a 2-micron film, indicating a volumetric capacitance density of 100 $\mu F /mm^3$, 10X higher than other current capacitor technologies.

CHAPTER 5

3D IPAC POWER MODULE: INTEGRATED L AND C

5.1 Introduction

This chapter it describes 3D IPAC (Integrated Passive and Active Components) power module substrate with integrated thinfilm inductors and capacitors. The 3D IPAC concept is based on an ultra-thin (30-100 microns) and ultra-low-loss glass substrate, low-cost and small through-package-vias (TPVs), thinfilm passives, and double-side redistribution layers (RDL) for assembly of both active and passive components. In this concept, the components are interconnected by means of these TPVs on both sides of the glass substrate, either as thinfilms or as discretely fabricated and assembled thin components, separated by only about 50-100 microns of interconnection length. This chapter specifically describes the 3D IPAC power module substrate by integrating thinfilm capacitors on one side and power-supply inductors on the other side.

Section 2 of the chapter describes the electrical modeling and design of power inductors and capacitors in 3D IPAC structure. Section 3 describes the fabrication of both these building block L and C components and their integration into a module. Section 4 presents the electrical characterization to demonstrate the benefits of 3D IPAC power modules.

5.2 Power Module Design

Typical power converter modules consist of an active power management IC (PMIC) along with an input decoupling capacitor, a storage inductor and an output filter capacitor. The required electrical performance determines the amount of capacitance and inductance. Therefore, electrical parameters such as maximum voltage and current ripple,

transient response, current handling, capacitor ESR and ESL, inductor losses are important in determining what passive components to use.

There are multiple methods to design power supplies with the required passive component values. One such method is using the target impedance of the complete power distribution system as a metric; another uses the tolerable ripple currents and voltages to calculate the component values. Both methods strive to reduce system noise and provide stable power supplies. The overall strategy then is to model and design the power module starting with component design, followed by interconnection parasitic extraction, optimization of component values, leading to a complete model of 3D IPAC module. This flow is shown in Fig. 5.1.

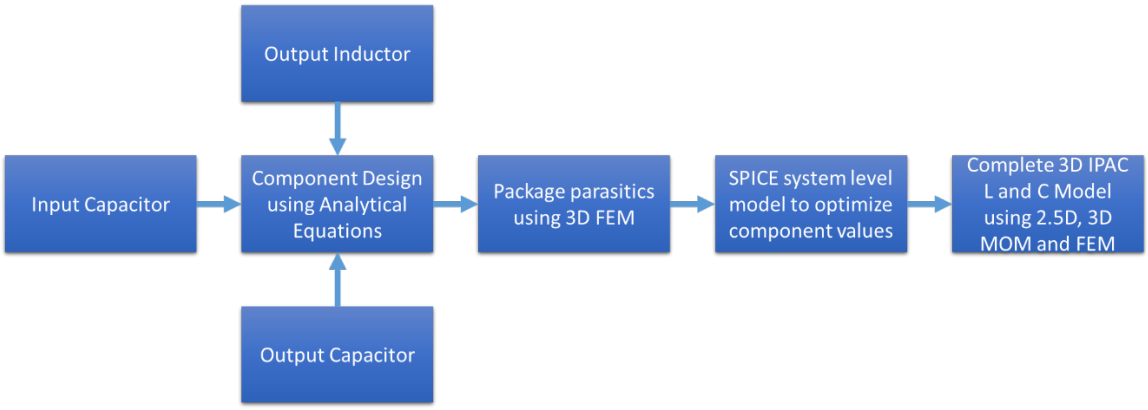


Fig. 5.1: Modeling and design strategy of the 3D IPAC power module.

5.2.1 Passive Components Design:

The following section presents the basic electrical models for designing passive components in power supplies with lowest ripple current and voltage, and improved efficiency. Fig. 5.2 shows the basic diagram of a buck converter[54]. The design of components for a buck converter with the required metrics is described next.

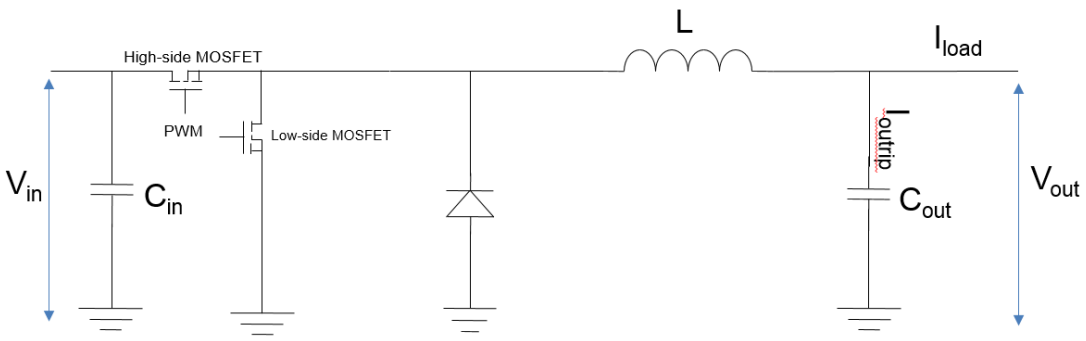


Fig. 5.2: Schematic diagram of a buck converter

5.2.1a Design of Input Capacitor:

The input capacitor (decoupling) is used to reduce the ripple voltage. This capacitor is placed as close to the PMIC as possible to reduce the parasitic loop inductance and provide high-frequency performance. Even a few nanohenries of inductance can be detrimental to the capacitor performance. It is important to select capacitors with the lowest possible equivalent series resistance (ESR). High ESR can lead to an increased voltage ripple at the input which results in a larger current ripples in the output. As a rule of thumb, the allowed voltage ripple can be assumed as 5 % of the required value. The following equations are used to calculate the value of the input capacitor:

$$I_{Inrip} = \frac{I_L}{2} \tag{5.1}$$

$$V_{inrip} = 0.05 * V_{in} \tag{5.2}$$

$$C = \frac{\Delta T}{\left(\left(\frac{Vinrip}{Iinrip}\right) - ESR\right)} \tag{5.3}$$

$$\Delta T = \frac{D}{F_{sw}} \tag{5.4}$$

$$D = \frac{V_{out}}{V_{in}} \tag{5.5}$$

Where, I_{inrip} is the input ripple current, V_{inrip} is the input voltage ripple, V_{in} is the input supply voltage, ESR is the equivalent series resistance of the capacitor, ΔT is the time period, D is the duty cycle, V_{out} is the output voltage and V_{in} is the input voltage.

5.2.1b Design of Storage Inductor:

The inductor value is chosen based on the required ripple current tolerance. The ripple current is ideally desired to be between 20 – 30% of the load current. The inductor value has to be chosen such that it can handle the peak load current. If it is unable to do so, this will result in a drop in inductance. This loss of inductance is generally due to core saturation. It is important to select an inductor core material with high saturation magnetization, low core loss and resistive loss to improve efficiency. High-value inductors are known to provide lower ripple current and lower hysteresis losses, whereas lower-value inductors can improve the transient response of the converter. The inductor design is related to the voltage and current as follows:

$$V = L\frac{\Delta I}{\Delta T} \tag{5.6}$$

Hence, the required inductance for the output filter of a DC-DC converter can be calculated as follows:

$$L = \frac{(V_{in} - V_{out}) * \Delta T}{I_{outrip}} \tag{5.7}$$

Where I_{outrip} is the output ripple current.

5.2.1c Design of Output Capacitor:

Selecting the right output capacitor is very important for a switching regulator. The inductor and capacitor form a second order low-pass filter. The capacitor value changes the cut-off frequency. It is important to make sure that the selected capacitor has low ESR, to reduce ripple voltage at the output than desired. The output capacitor impedance also affects the feedback loop. Hence, it is important to understand the required target impedance for the entire power distribution system. The capacitor is related to the voltage ripple and current as follows:

$$I = C\frac{\Delta V}{\Delta T} \tag{5.8}$$

Hence, the required capacitance for the output filter of a DC-DC converter is calculated as follows:

$$C = \frac{(I_{outrip} * \Delta T)}{\Delta V - (I_{outrip} * ESR)} \tag{5.9}$$

The above equation assumes that the equivalent series inductance (ESL) of the capacitor is extremely small and does not affect the output filter performance.

All of the above equations can be used to calculate the minimum required values. Hence, it is important to select components of values larger than those provided by the above analysis. Table 5.1 provides the design metrics for the 3D IPAC power module.

Table 5.1: Target metrics for the power module

Metric	Target
V_{in}	3 V
V_{out}	1.2 V
I_L	500 mA

Hence, using Equations 5.1-5.9 from Section 2.2, we get

I_{inrip} = 250 mA

V_{inrip}= 150 mV

F_{sw}=100 MHz

I_{outrip}=100 mA

D= 0.4

ΔT= 4 ns

Hence,

$C_{in} = \frac{4e-9}{\left(\frac{150}{250}\right)-0.1}$ = 8 nF

$L = \frac{1.8*4e-9}{100e-3}$ = 72 nH

$C_{out} = \frac{100e-3*4e-9}{50e-3-(100e-3*0.1)}$ = 10 nF

5.2.2 Modeling of Package Parasitics:

The package parasitics determine the overall module performance. Q3D extractor and HFSS were used to extract the 3D IPAC package parasitics as s-parameter data, with different TPV size and locations. Lowest loop inductance was achieved by optimizing the

total number of TPVs, the location of TPVs, the placement of integrated components and plane thickness. The plane thickness and dimensions were also optimized for lowest plane resistance.

A modeling methodology was setup to study both the time and frequency domain response of the interconnection parasitics in a 3D IPAC structure. Fig. 5.3 shows the methodology used. S-parameters from HFSS were obtained based on the required frequency sweep. The R, L and C were then extracted from the S-parameter data. Table 5.2 provides a comparison of the R, L and C data between traditional packaging technologies and 3D IPAC. It is evident from the table that 3D IPAC has the lowest package parasitics than any package today.

The R,L and C values obtained from the modeling were used in a linear spice model of a VRM [54]. A single modeling step was required to obtain both the input and output package interconnect parasitics. The time-domain output was plotted using ADS and LTSPICE. The results clearly show the improved performance of the 3D IPAC power module over traditionally -packaged modules. The reason for such a huge improvement in performance is the lower parasitic inductance and resistance that is achieved when using the 3D IPAC concept. Fig. 5.4 shows the time domain response.The 3D IPAC has lower impedance over a broad range of frequencies. Hence, with the appropriate passive components, the required target impedance can be met at frequencies greater than 100 MHz.

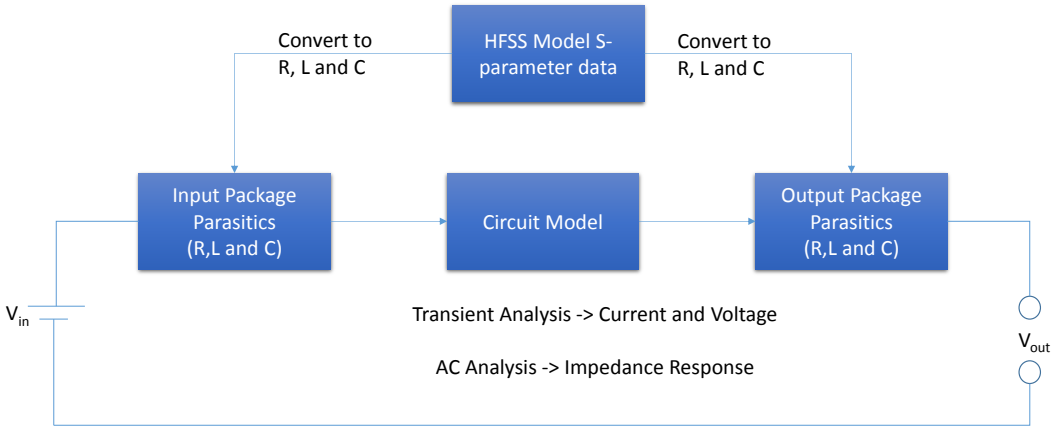


Fig. 5.3: Electrical modeling strategy, shown here as a simple circuit schematic for SPICE simulations.

Table 5.2: Comparison of R, L and C for different package types

	Resistance (Ohms)	Inductance (nH)	Capacitance (pF)	Operating Frequency (MHz)
Wirebond LF Packages	>0.04	0.85 – 1	0.3 – 0.35	0.02 – 0.5
Micro BGA Packages	>0.01	0.2 – 0.5	0.1 – 0.20	0.5 – 2
3D IPAC(L and C)	<0.005 – 0.01	0.02 – 0.1	< 0.05	> 100

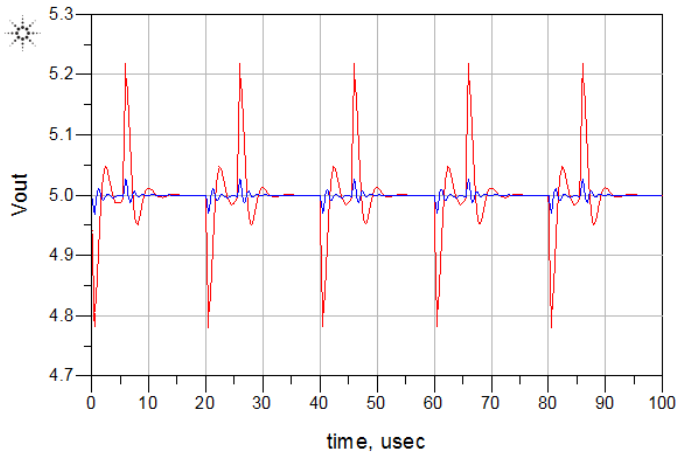


Fig. 5.4: Performance improvement of 3D IPAC Vs. traditional packages.

5.2.3 Complete Circuit Design of 3D IPAC Power Module:

The complete circuit design involves passive components and the package parasitics. Design analysis was performed to achieve the target module specifications compiled in Table 5.1. The values obtained from the analytical design study (Section 2.1) and parasitics modeling (Section 2.2) were used to model and simulate test circuits to obtain the most optimum design. The test circuit, seen in Fig. 5.5, represents a simplified model for buck converters. Most state-of-art buck converters employ a two-transistor design with one high-side MOSFET and one low-side MOSFET. A voltage-controlled switch was used to model an ideal switching transistor without any parasitics. This helps to greatly simplify the modeling process and focus on the passive component selection and design. As a first step, the model was simulated without any output (package) parasitics. The results are as seen in Fig. 5.6.

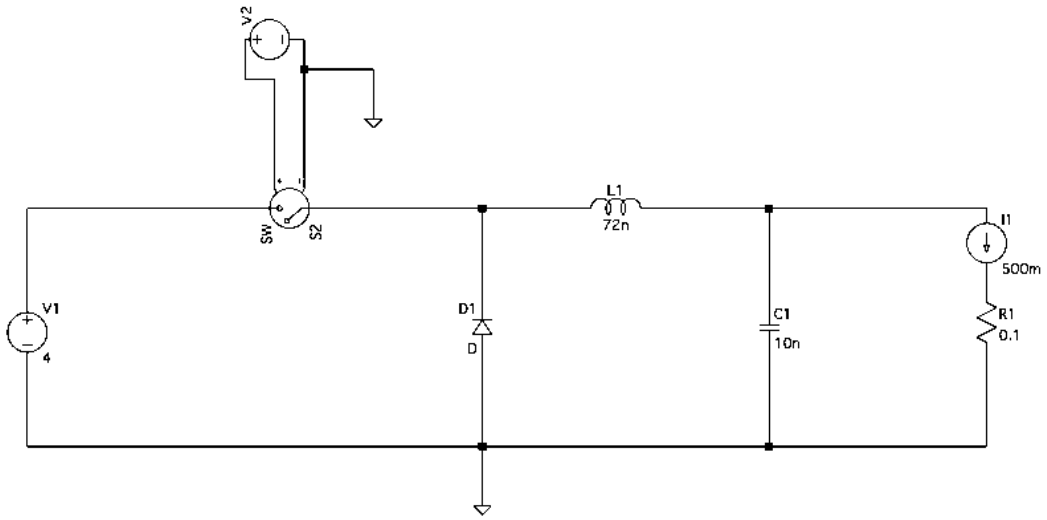


Fig. 5.5: Simplified schematic of a buck converter

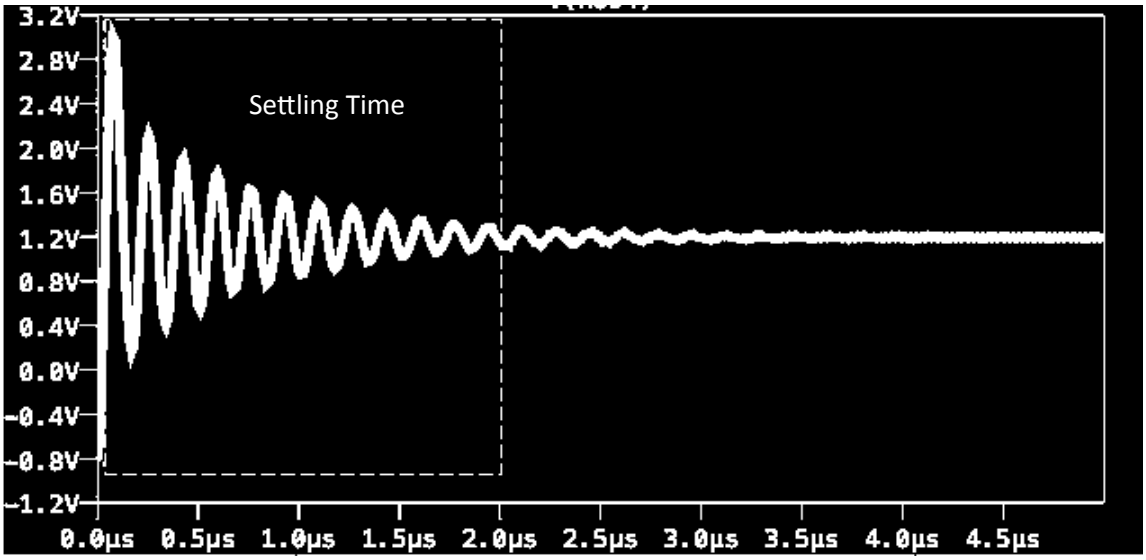


Fig. 5.6: Simulated output voltage with designed passive components and no parasitics.

The simulation results show a large settling time of almost 2 µs compared to the relatively small 10 ns time-period. However, after 2 µs, the output voltage ripple settles to within the required targets. Fig. 5.7 shows the ripple voltage after 2 µs.

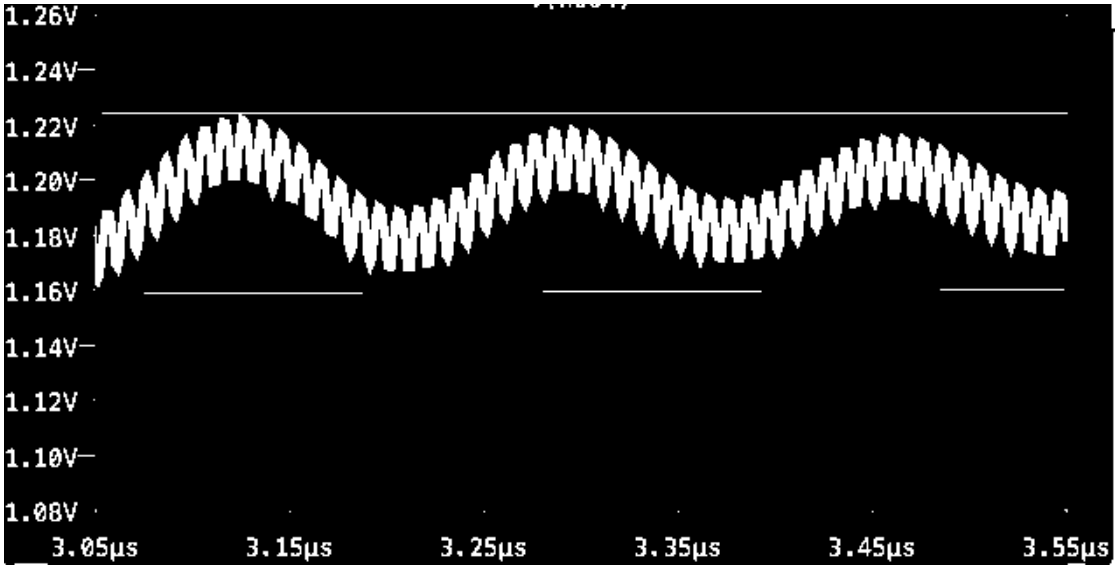


Fig. 5.7: Voltage ripple of less than 30 – 40 mV after a settling time of 2 µs

To better understand the system design, the model was simulated once again with all the package parasitics included. A total inductance of 1 - 4 nH was used to simulate state-of-art 2D packages whereas an inductance 150 pH was used for the 3D IPAC structure. The parasitic inductance for 3D IPAC is much lower compared to state-of-art packages because of the ultra-short vertical interconnections and proximity to the active ICs. Fig. 5.8 shows results with the designed input capacitor and inductor values and added parasitics. In both cases, the ripple voltages are much higher compared to the first case (without any package parasitics) and do not meet the target requirements. Even with the significantly lower parasitic inductance of 3D IPAC, the ripple voltage is almost 300 mV.

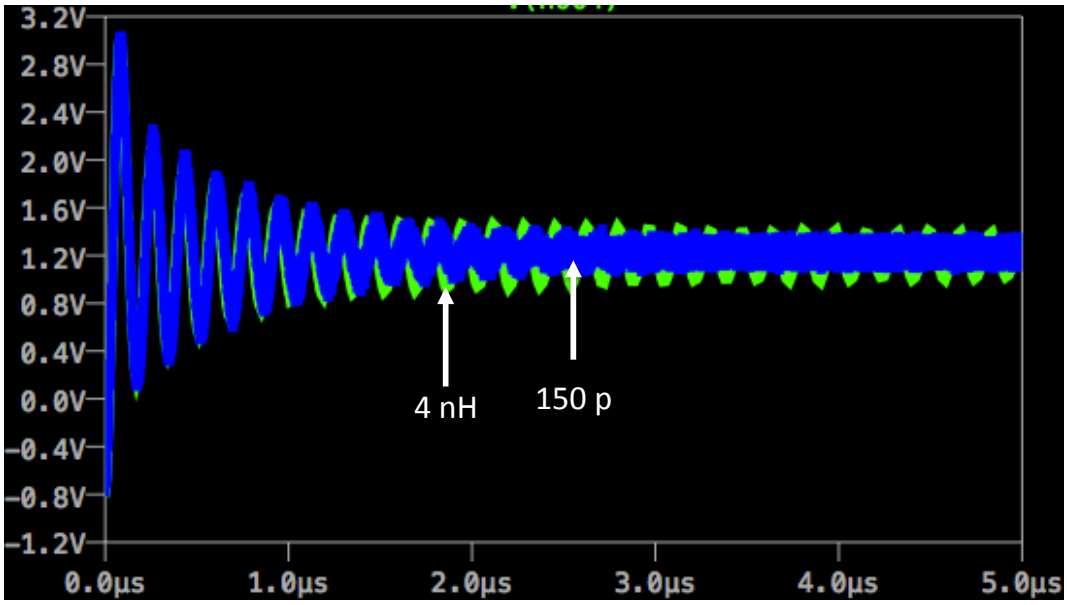


Fig. 5.8: Output voltage ripple with 4 nH (State-of-art) and 150 pH (3D IPAC) parasitic inductances.

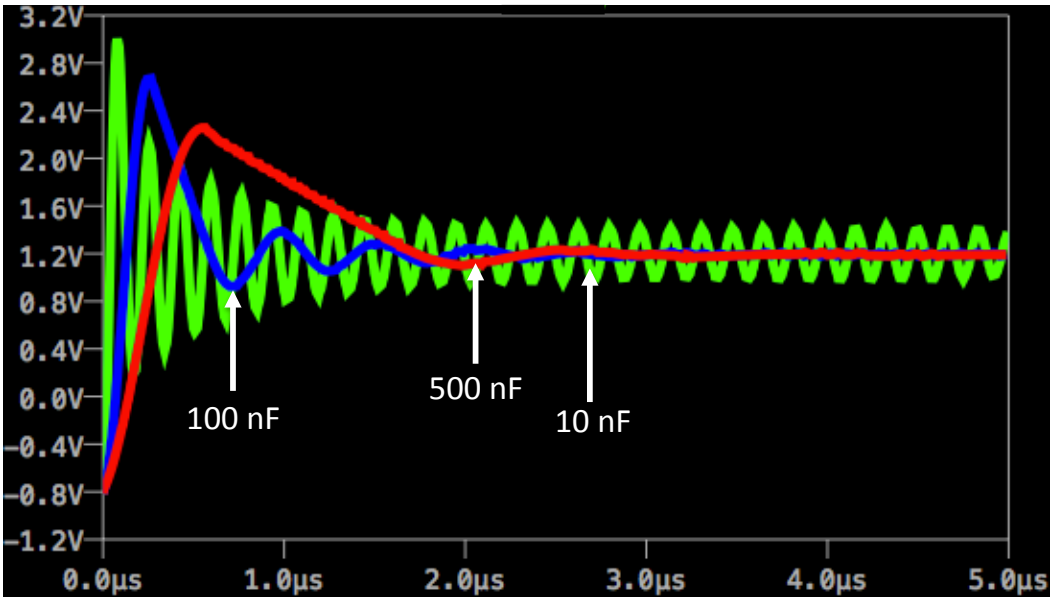


Fig. 5.9: Output voltage ripple with 10, 100 and 500 nF capacitors.

To improve the design and meet the target specifications, parametric studies were performed with different output capacitors. Fig. 5.9 shows results from three simulations of this study. The results show that a capacitor of 10 nF has a large ripple voltage (400 mV) at the output whereas the 500 nF and 100 nF capacitors meet the target specifications. The higher capacitance results in a lower voltage spike but it also has a slower ramp down because of the larger RC time constant. This makes 100-nF capacitors more attractive for this application. Smaller capacitances (100 nF) can be easily achieved using high-density Ta capacitors (100 $\mu F/cm^2$) integrated using the 3D IPAC approach in an area of ~ 0.1 mm^2.

5.2.4 Full 3D model of 3D IPAC with L and C:

Full 3D Electrical modeling and design is essential to get the optimum performance from the power modules. Modeling was performed to study the electrical characteristics of inductors and capacitors when fabricated on the same side of the substrate versus when they were fabricated as double-side components separated by ultra-thin glass.

The required inductance and capacitance values were based on voltage ripple requirements, transient response and current handling. Multiple geometries were considered to obtain the required inductance. A 2.5D MOM solver, SONNET SUITES, was used as the modeling software. The tool provides fast and accurate results in the frequencies of interest (between 100 – 500 MHz).

The inductors were modeled as single-layer RDL structures. They provide the best performance in inductance density, Q-factor and frequency performance. The polymer core (ZIF – ZEON Chemicals) had an extremely low-loss of 0.005. Table 5.3 provides results obtained from 2 x 2 mm^2 and 3 x 3 mm^2 inductors modeled on ultra-thin glass substrates. The table compares the inductance and Q-factor obtained for various metal thicknesses.

Table 5.3: Inductance and Q-factor for single layer air-core inductors based on area and metal thickness

Area	Thickness (μm)	Inductance (nH)	Q-factor
2 x 2 mm^2	10	90	25
	20	83	36
	30	82	35
3 x 3 mm^2	10	82	32
	20	81	48
	30	80	45

The capacitors were modeled as simple parallel-plate structures. The Ta_2O_5 layer forms the dielectric. Dielectric thickness of 24 nm was used in the modeling study. To get accurate results, the inductors and capacitors were simulated on either sides of the glass substrates, interconnected using through vias. A marked improvement in performance was noted when compared to the scenario where they were both simulated on the same

side of the substrate, as depicted in Fig. 5.10. The complete 3D IPAC targets are seen in Table 5.4.

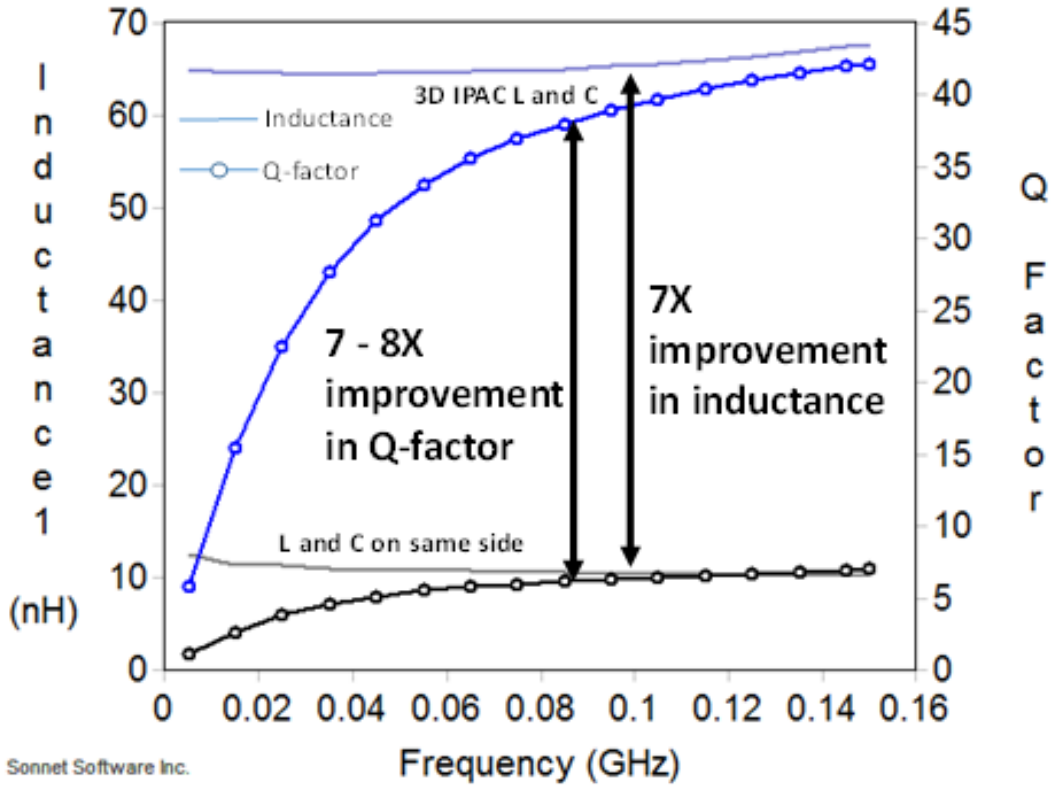


Fig. 5.10. Inductance and Q-factors obtained from modeling 2 x 2 mm^2 air-core inductors using SONNET. 3D IPAC shows 7X improvement in inductance and 7-8X improvement in Q-factor compared to both components fabricated on the same side of the substrate.

Table 5.4: Targets for 3D IPAC Power Modules with Integrated L and C

Parameter	Prior Art	Targets	Challenges
• Module dimensions (mm^3)	• 2.9x2.3x1	• 2x1x0.15	• 3D integration of ultra-thin components • TPVs in glass
• Loop Inductance (nH)	• 1 – 10	• < 0.2	• Interconnect length in Z and X-Y directions
• Integrated Capacitor ($\mu F/cm^2$)	• 1 – 2	• 100	• Ultra-thin component integration on ultra-thin substrates
• Integrated Inductor (nH)	• 20 – 30 • (Q <20)	• 80 • (Q>35)	• Integration using single layer RDL on ultra-thin substrates
• Frequency (MHz)	• 1 – 2	• >100	• Component stability > 100 MHz

5.3 3D IPAC Fabrication with Integrated L and C

The proposed 3D IPAC functional module requires the integration of multiple building block technologies such as capacitors and inductors. This section focuses on the fabrication of ultra-thin glass substrates with: 1) Single-layer RDL for power inductors, 2) High-density Ta and thinfilm capacitors, and 3) 3D IPAC fabrication with integrated L and C. The first two items deal with the building blocks, while the last item deals with the module demonstration.

5.3.1 Single layer RDL Power Inductors:

The main focus of this task is to fabricate integrated power inductors using single RDL layers. In this approach, ultra-thin glass substrates were laminated with ultra-low-loss polymer (ZIF – ZS100) using a vacuum lamination process. Next, a seed layer of Cu was electroless-plated. This was followed by photolithography to define the spiral inductor

structures. Electroplating was used to create the required patterns up to 20 μm Cu thickness. Finally, the seed layer was etched to form the complete inductor structures. All of the above processing was performed using panel-compatible processes. Fig. 5.11 shows the complete inductor fabrication process using SAP (Semi-additive patterning). An optical image of the fabricated inductor is seen in Fig. 5.12.

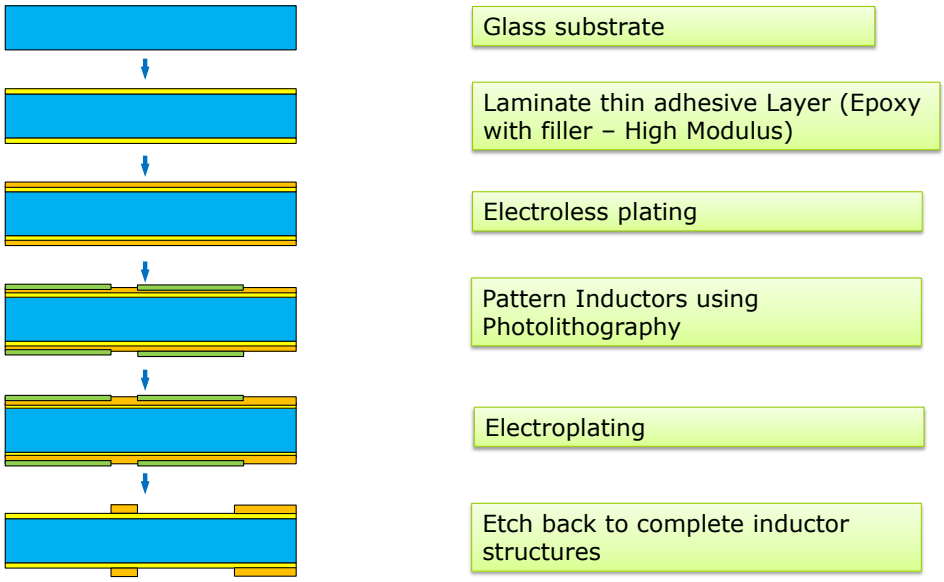


Fig. 5.11. Fabrication process for polymer-core inductors on ultra-thin glass substrates.

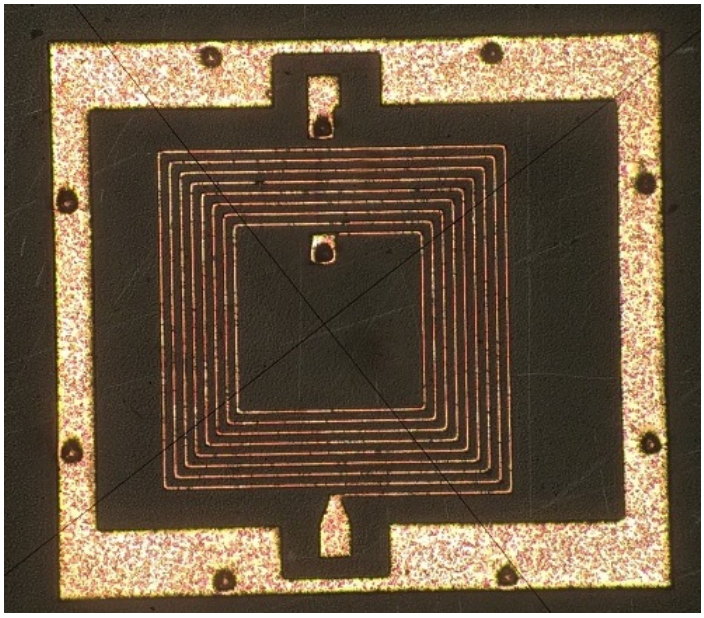


Fig. 5.12. Polymer-core inductors fabricated on ultra-thin glass substrates.

5.3.2 High-Density Ta and Thinfilm Capacitors

High-density Ta capacitors with ultra-high surface area were fabricated on Ta foils. Thinfilm capacitors with sputtered tantalum followed by anodization were also fabricated. These capacitors were laminated onto ultrathin glass substrates using polymer adhesive layers. The following are the steps used to integrate the capacitors. Fig. 5.13 shows the representative process flow.

- Pre-fabricated capacitor foils were laminated onto the glass substrate using (ZIF – ZS100) with a vacuum lamination step
- The same ZIF polymer was also used as a planarization layer
- A laser via process was used to drill blind vias onto both the anode and the cathode
- Photolithography was used to define the interconnections on the top surface to complete the capacitor fabrication.

The fabricated capacitors are shown in Fig. 5.14.

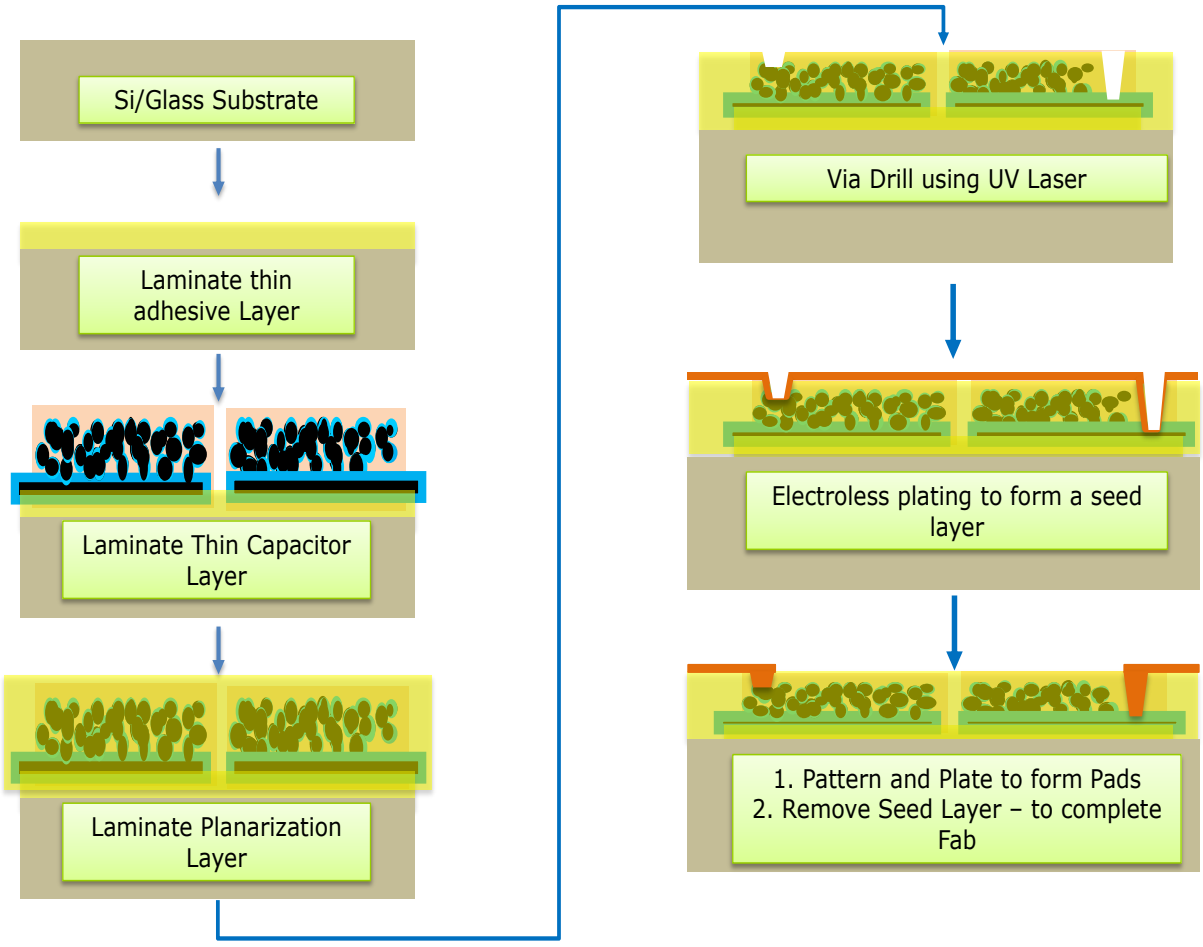
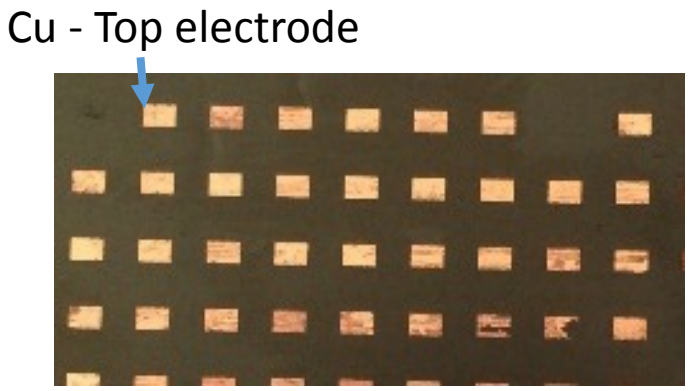


Fig. 5.13. Ultra-thin high-density capacitor using foil-transfer on ultra-thin glass substrates.



(a)

(b)

Fig. 5.14. (a) Foil-transferred Ta capacitors on ultra-thin glass substrates and (b) Blind via drilled to expose the cathode.

5.3.3 Complete 3D IPAC Fabrication with Integrated L and C

The primary objective of this research is to design and fabricate 3D integrated passive and active components with the building blocks, described above. The module design consists of ultra-thin high-density capacitors integrated on one side and interconnected with power inductors on the other side with TPVs. Fig. 5.15a shows the complete panel-level layout. Unit structures containing both the inductor and capacitor layers are seen in Fig. 5.15b and 5.15c respectively. The inductors used in this process were the same as described previously in Section 2.2b. However, the capacitors fabricated in the integration process were based on thinfilm silicon oxide. They were chosen for process demonstration because of their relatively simple process steps compared to Ta.

The 3D IPAC fabrication process involves the following key steps:

- Ultra-thin glass substrates with through-package vias
- Fabrication of thinfilm capacitors on one side
- Power inductor fabrication on the other side
- Blind-via formation to form the required interconnections
- Via plating and top layer patterning to complete the LC structures.

Fabrication of glass substrates with 2-ML was developed at GT-PRC as a part of its glass substrate program. This is a modified version of the standard semi-additive process (SAP) where plating is accomplished on both sides at the same time. However, to achieve thinfilm capacitors with silicon dioxide as a dielectric on one side and polymer-core inductor on the other side, further modification to the SAP process flow is required. This involves simultaneous double-sided electroless seeding and electroplating and is described in Fig. 5.16.

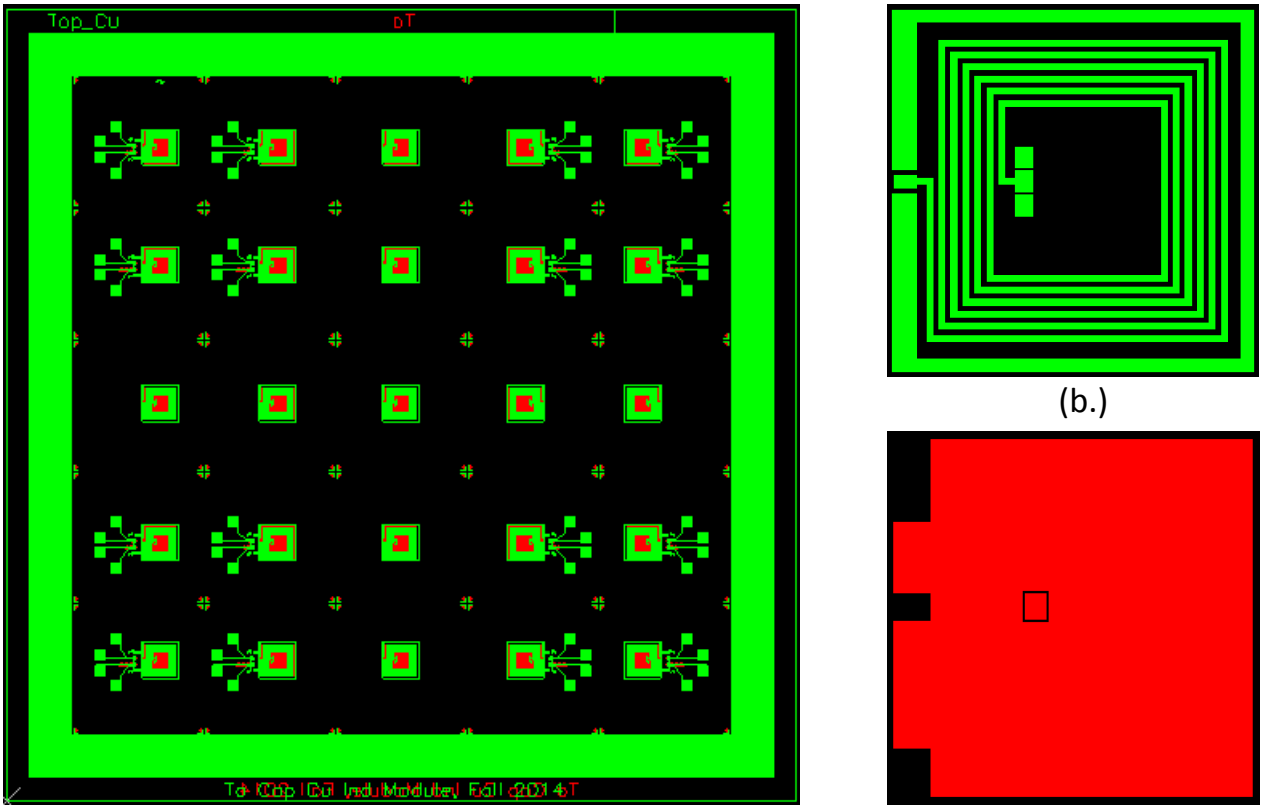


Fig. 5.15. Complete design of the 3D IPAC L and C modules: (a) Panel level view – 6" x 6" panel with 2 x 2 mm^2 L C modules, (b) A unit design of the capacitor, and (c) Unit design of the inductor structure.

This process utilizes ultra-thin glass substrates of 130μm thickness from corning glass. These substrates had pre-fabricated through package vias. The glass samples were first cleaned using acetone, methanol and isopropyl alcohol and baked at 120 C for 30 minutes. Next, silane treatment was applied to improve the adhesion of the polymer to the glass substrate. The ZIF polymer film was used as build-up material. It was laminated using a vacuum laminator. A temperature of ~ 93 C is required to achieve void-free

lamination. Next, a hot press was used at ~ 115 C with a pressure of 2 tons to improve the adhesion. The samples were then annealed at 180 C for 60 mins in nitrogen.

A CO_2 laser was used to rework the vias in the polymer-laminated glass in select areas. Next, seed layer was formed on top of the polymer-laminated glass using electroless plating. This forms a continuous electrical contact across the panel, which is required for the electrolytic plating step, after photolithography. As part of the electroless plating step, a desmear process is required to increase the surface roughness of the polymer for improved adhesion of the electroless plated Cu. Table 5.5 describes this process step-by-step. Fig. 5.17 shows an electroless plated glass sample.

Table 5.5: Desmear process flow required for e-less plating on polymer build-up.

Step Number	Process	Function
1	Sweller	Swelling resin to ease the removal of smear by permanganate bath
2	Rinse	
3	Permanganate	Oxidize smear to be removed and roughen the surface of the polymer
4	Rinse	
5	Reducer	Reduce remaining permanganate on a surface
6	Rinse	

The L and C patterns were then defined on both sides of the ultra-thin glass using photolithography. The mask patterns are shown in Fig. 5.15. Samples with L and C patterned, with TPVs is seen in Fig. 5.18. Negative tone dry films were used as the photoresist. After exposure and development, plasma descum process is required to rid the sample of any resist residue in the patterned areas. Copper was electroplated after the plasma descum process. Finally, the photoresist was stripped and the seed-layer etched to complete the inductor structures and bottom electrodes of the capacitor.

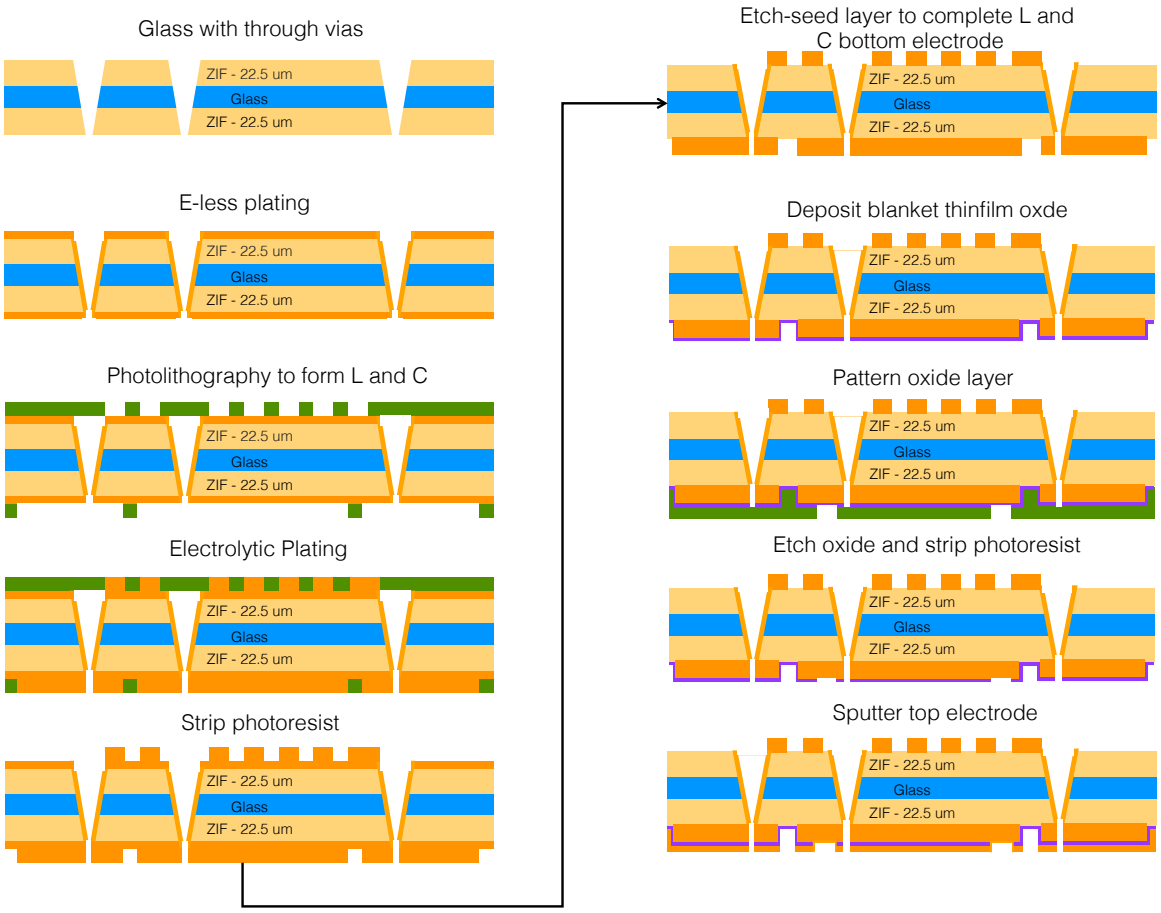
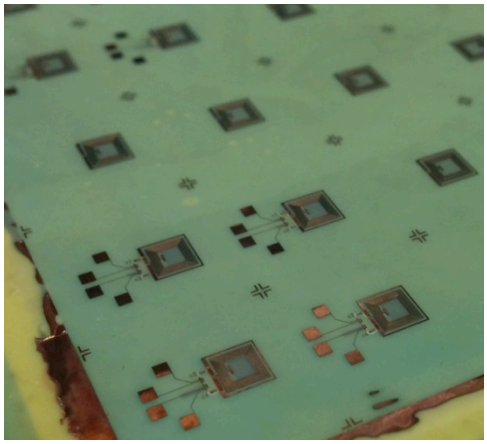


Fig. 5.16: Modified process flow for power L and C on glass using SAP.

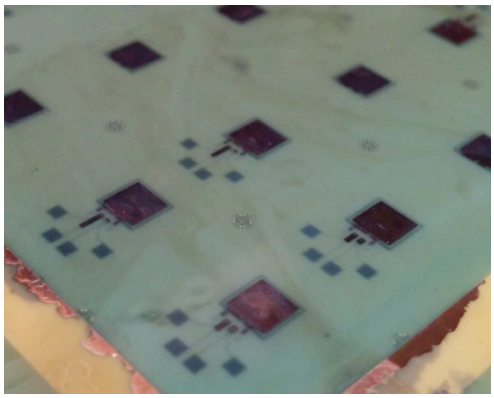
The samples required further processing to complete the thinfilm capacitor structure. This involves formation of the dielectric and top electrode. Silicon dioxide was selected as the primary dielectric. Plasma-enhanced chemical vapor deposition (PECVD) technique was used to deposit the oxide. Standard PECVD oxide deposition utilizes a platen temperature of 250 C. However, the recipe was modified to work with a platen temperature of 150 C for the polymer-laminated glass.

Fig. 5.17: E-less plated Cu on glass

The capacitor design and fabrication process was relatively more complex than the inductor. A small keep-out zone was required such that the TPV from the inductor could only connect to the top electrode whereas the others connected only to the bottom of the capacitor. To connect the top electrode to the inductor, blind-vias had to be fabricated in the oxide dielectric layer. Sputtering was used to metallize the top-electrode layer to complete the fabrication process. Fig. 5.19 shows the bottom plates with keep out zone. Fig. 5.20 shows the patterned microvias.



(a.)



(b.)

Fig. 5.18: Complete fabricate 3D IPAC L (a.) and C (b.)

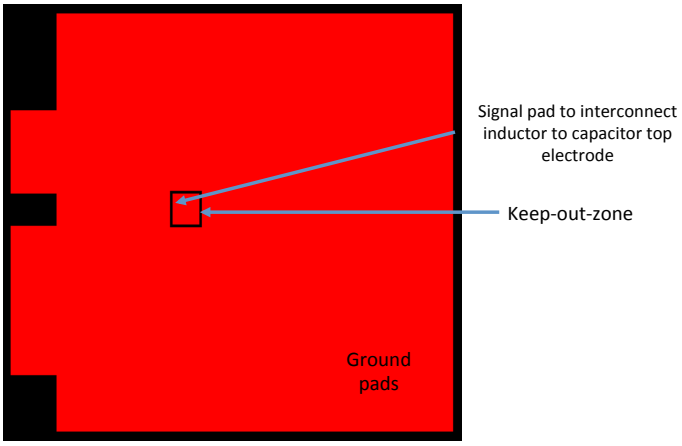


Fig. 5.19: Bottom electrode of the capacitor showing keep-out zone, signal and ground regions.

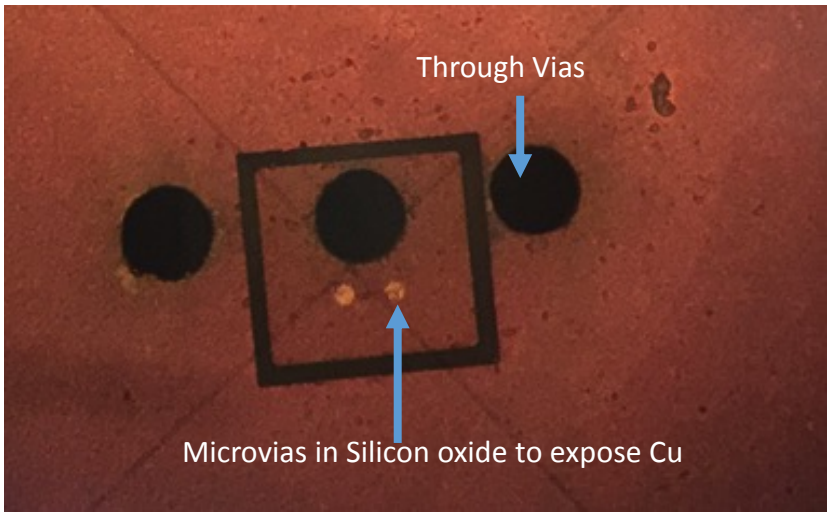


Fig. 5.20 Micro-vias drilled in silicon dioxide dielectric.

5.4 Electrical Characterization

Characterization of the individual components is performed to understand the model-to-hardware correlation. This helps to validate the inductor and capacitor structures, and set the design rules for the integrated 3D IPAC L and C module.

The capacitors were characterized using an HP LCR meter. A capacitance density of 3.3 nF/mm^2 was achieved with the planar Ta capacitors anodized at 8V. These results, due to different anodization voltages, are presented in Table 5.6. The leakage current was found to be less than 1 nA/nF at 3V for the samples anodized at 8V. These results indicate the formation of a very good dielectric layer with minimal defects. The silicon dioxide capacitors fabricated as a part of the 3D IPAC approach were tested using the same method. A capacitance density of 0.7 nF/mm^2 and leakage current of 1 nA/nF were achieved. As an alternative approach, Al_2O_3 Capacitors were also fabricated on ultra-thin substrates using atomic layer deposition. Dielectric films of under 20 nm were obtained

almost defect free. The dielectric constant of alumina is ~ 9. These capacitors showed 1.2 nF for 0.28 mm^2 device. This translates to a capacitance density of 6 nF/mm^2, which is a 10X improvement over silicon dioxide.

The inductors were measured using a vector network analyzer (VNA). SOLT calibration was used to calibrate the system to measure the required low-frequency data. The VNA provide the s-parameter data. The inductance extracted from the s-parameters versus the modeled inductance is presented in Fig. 5.21. The results indicate good correlation between the modeled and the measured data.

Table 5.6: Capacitance Density and Breakdown Voltage as a function of Anodization Voltage for thinfilm Ta capacitors.

Anodization Voltage (V)	Capacitance Density (nF/mm^2)	Breakdown Voltage (V)
8	3.3	5
60	1	30

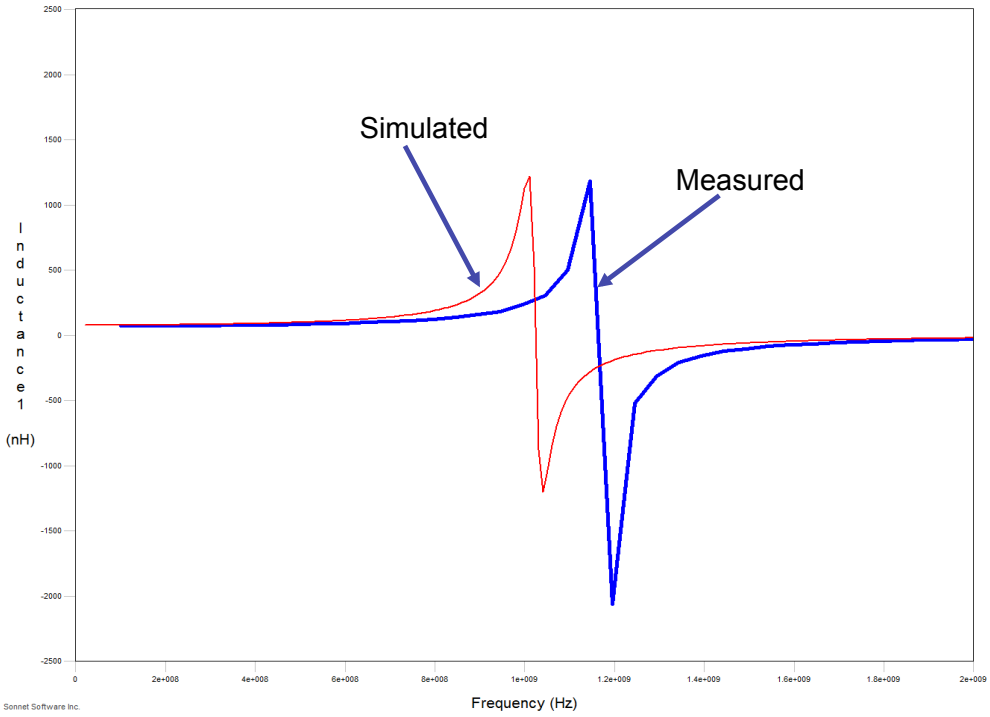


Fig. 5.21. Hardware-Model correlation for integrated polymer-core inductors on ultra-thin glass substrates.

The complete 3D IPAC structures fabricated with inductor on one side and capacitor on the other of glass substrates, interconnected with through-vias were characterized using a VNA. The measurement process was similar to the one used to measure the inductor structures. Fig. 5.22 shows a 3D IPAC structure under test. The measured results are seen in Fig. 5.23. The L and C were designed to have a low-pass filter response at 100 MHz. The data shows good correlation to the designed filter response.

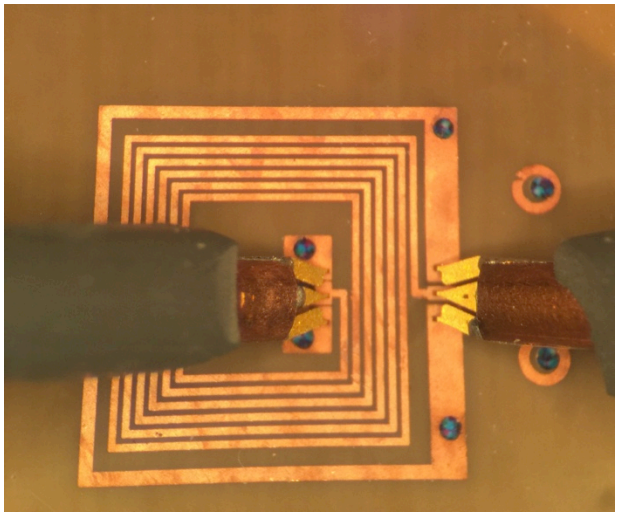


Fig. 5.22: A 3D IPAC L and C under test using a vector network analyzer.

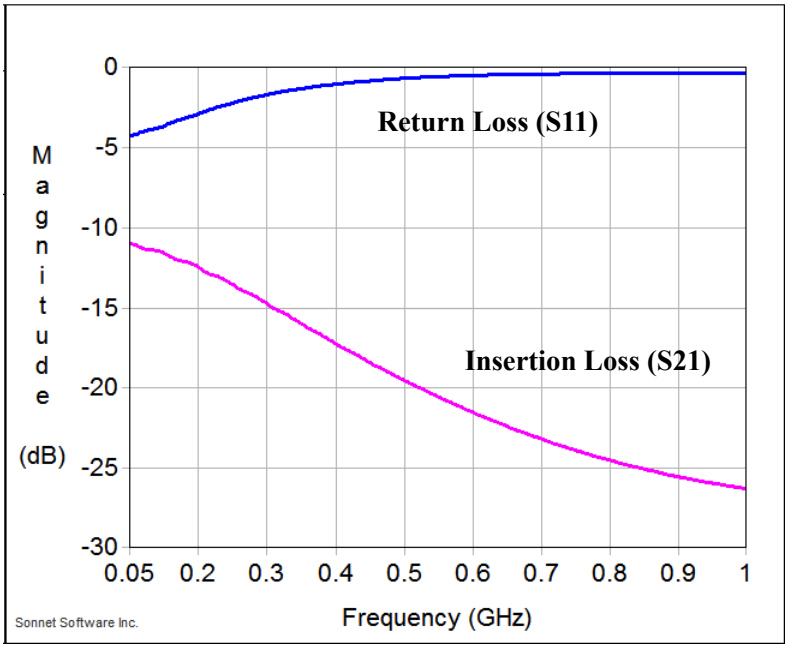


Fig. 5.23: S-parameter measurement showing low-pass filters response at 100 MHz for 3D IPAC L and C.

5.6 Summary:

An innovative 3D IPAC power module concept using ultra-thin glass and through-vias and with advanced and integrated inductors and capacitors is presented. The benefits of 3D IPAC with integrated L and C concept was demonstrated by modeling with Ta capacitors and single-layer RDL inductors. Individual technologies to integrate both thinfilm high-density capacitors and inductors were developed on ultra-thin glass substrates. A 3D IPAC power module emulator with integrated L and C was designed and fabricated.

A variety of capacitors were explored to demonstrate the 3D IPAC concept. These include tantalum oxide capacitors, which showed high-yield (> 90%) with very low leakage current < 1 nA/nF at 3V. These results indicated that the dielectric film was almost defect-free. A capacitance density of 3.3 nF/mm^2 was achieved with an anodization voltage of 8V. The second capacitor was based on ALD alumina dielectric of 20 nm with a capacitance density of 6 nF/mm^2. Capacitors fabricated as part of the 3D IPAC integrated L and C approach showed capacitance densities of 0.7 nF/mm^2. Air-core inductors were designed and fabricated to achieve 80 nH with a Q-factor >35 at 100 MHz. A 7X improvement in inductance and a 7-8 X improvement in Q-factor were demonstrated in the 3D IPAC structure with components on both sides of the glass and interconnected with through vias, compared to the state-of-the-art where components are assembled on the same side.

A complete power LC network with double-side thinfilm components was fabricated and tested to validate the electrical models. The 3D IPAC concept with miniaturized and low-cost power components to form the most advanced power modules starts a new era to address the strategic need for ultra-miniaturized power modules.

CHAPTER 6

SUMMARY AND OUTLOOK

6.1 Research Summary

Low-power modules for consumer (0.5 – 5 W) typically consist of power management ICs combined with input capacitors, output storage inductors and output filter capacitors for achieving the output voltage and current levels within the tolerance for the devices. In today's smart systems, such power modules are manufactured with SMD passives and discretely-packaged actives that are mounted on the board, far from the active ICs. This increases the interconnect parasitics and reduces performance. The proliferation of multi-functional smart systems with multiple such point-of-load power converters further aggravates this problem by multifold, creating a major bottleneck for system miniaturization and performance enhancement.

One approach to meet the miniaturization and performance needs is to improve the frequency performance of the power module. This leads to reduced inductance and capacitance. It also helps in reducing the need for passive components all over the power supply network. However, this requires several advances in passive component technologies such as high quality factors, thinner form-factors and ultra-thin substrates with ultra-short interconnections.

This study investigates an innovative 3D integrated actives and passives (3D IPAC) package concept with advanced thinfilm passive components to address power supply module miniaturization. The 3D IPAC approach aims at integrating PMICs with high-density capacitors and inductors interconnected by ultra-short through package vias on ultra-thin glass substrates.

The first part of the study investigates advanced capacitor technologies. High-k thinfilm capacitors using barium strontium titanate dielectrics with lanthanum nickel oxide electrodes were demonstrated in 3D IPAC concept in glass with glass-compatible temperatures and processes. A capacitance density of 30 nF/mm^2 was achieved with leakage currents of 1-10 nA/nF up to 3 V.

Another capacitor approach using Si-nanowire capacitors were also investigated as an alternative approach to planar capacitors. In contrast to high-permittivity thinfilm capacitors, these achieve higher capacitance density due to higher electrode surface area. Nanowires were fabricated on Si using both CVD and wet-etching processes. These capacitors with SiO_2 dielectrics showed densities of 200 nF/mm^2. This is a 40 X enhancement, compared to planar capacitors with 50 nm dielectrics. It is estimated that the nanowire capacitors will be limited in frequency to a few kHz. This is attributed to the high resistance of the nanowires coming from the silicon wafers (1-10 ohm-cm resistivity). With low-resistivity (highly-doped) Si capacitors, the frequency response can be improved. Another approach to achieve improved frequency response with even higher capacitance is to use atomic layer deposition. TiN and Al_2O_3 can be deposited using ALD as an electrode and dielectric respectively to achieve improved performance. This will also help eliminate the need for specific bias voltages to achieve maximum capacitance.

The second part of the study focused on integrating L and C using the 3D IPAC package concept. As a first step, electrical modeling was performed to understand the benefits of the approach. Modeling of the substrate showed minimum parasitic inductances leading to lowest voltage ripple performance at the output when compared to state-of-art power modules. The L and C structures were modeled using SONNET 2.5 D MOM solver

showed improvement in performance (7X higher inductance and Q-factor) with 3D IPAC package structure relative to when the structures were fabricated on the same side of the substrate. Fabrication processes were developed for individually integrating L and C using ultra-thin glass substrates. Finally, a 3D integrated module was designed, fabricated and characterized. The fabricated samples showed good correlation to the modeling data.

6.2 Future Work

The following directions are suggested for future research:

6.2.1 Barium Strontium Titanate thinfilm capacitors:

- Explore different barrier materials and electrodes for lower diffusion rates at high anneal temperatures, resulting in improved interfaces: This could help achieve higher densities, lower leakage currents and higher breakdown voltages.
- Study the electrical benefits of integrating ultra-thin high-k thinfilm BST capacitors with LNO electrodes on ultra-thin glass interposers: Due to the proximity to the actives and ultra-short interconnections the capacitors could be operated at much higher frequencies compared to state-of-art decoupling schemes.
- Explore the fabrication processes required to integrate such capacitors on ultra-thin interposers and substrates: Embedded and 3D IPD decoupling have met with limited success because of the complexity of processing and the relatively higher fabrication cost. This makes alternative low-cost fabrication processes and electrodes highly desirable.

6.2.2 Si-nanowire capacitors:

- Explore higher-conductivity Si-substrates for improving the overall frequency response: The current study focused on using test wafers (1 – 10 ohm-cm) with relatively high resistivity resulting in limited frequency response. It was estimated that the capacitors would be limited to a few 10's of kHz. Higher-conductivity Si can be used to mimic the behavior of metal electrodes leading to higher frequency performance.
- Study the use of alternative dielectrics such as hafnia, alumina, titanium oxide, etc. using atomic layer deposition (ALD): A fabrication process that can achieve conformal deposition of such dielectrics on the high aspect-ratio Si-nanowire structures can help achieve much higher capacitance densities.
- Explore multiple layers of electrodes and dielectrics to enhance capacitance densities: One such approach could use layers of TiN and Alumina. This structure would behave as several MIM capacitors connected in parallel leading to even higher capacitance densities relative to the high conductivity SIM capacitors.

6.2.3 3D IPAC with L and C:

- Enhance current fabrication processes beyond polymer-core inductors and thinfilm capacitors: Integrating high-density Ta capacitors and high-density inductors with magnetic cores can improve power module performance and help eliminate multiple passive components on the package and board.
- Study the reliability of integrated modules: 3D IPAC with integrated high density L and C on ultra-thin glass substrates requires multiple building block technologies to come together. Hence, reliability can be a major challenge. Studying and characterizing failures can help improve designs and fabrication processes leading to highly reliable modules.

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